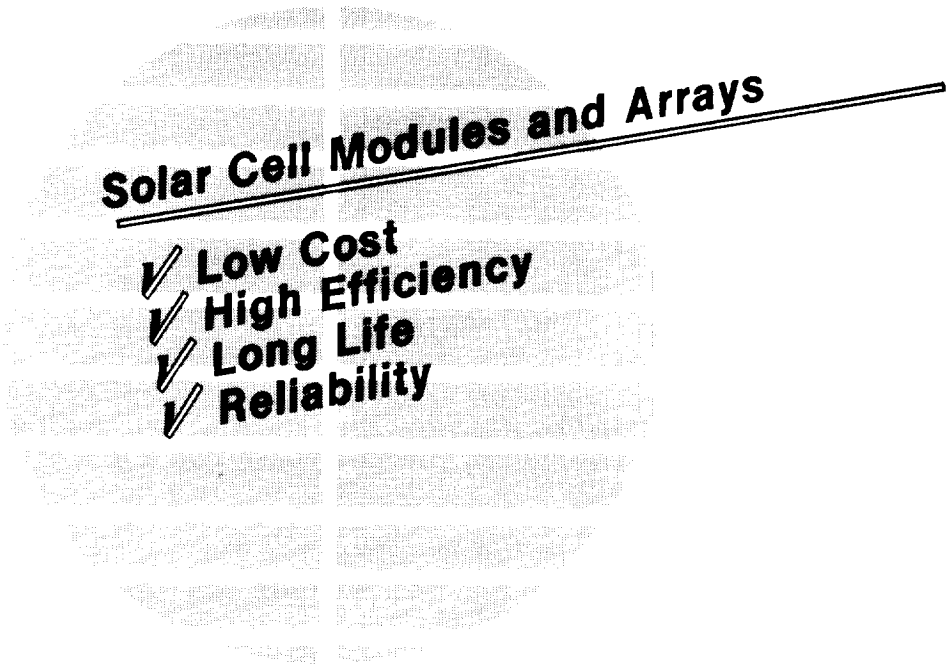
JPL Publication 86-31

Electricity from Photovoltaic Solar Cells

Flat-Plate Solar Array Project Final Report

Volume V: Process Development

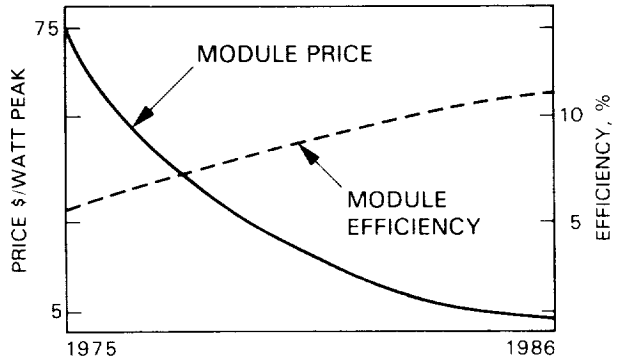
11 Years of Progress



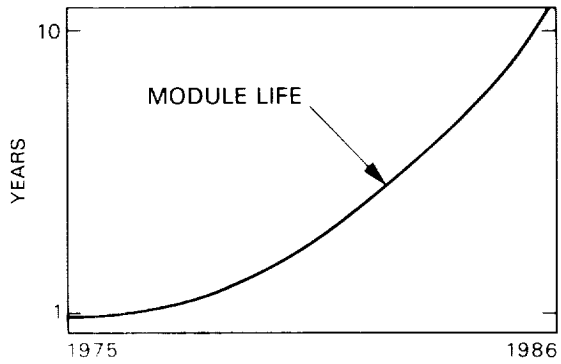
October 1986

Project Managed by the Jet Propulsion Laboratory for the U.S. Department of Energy

Photovoltaic Module Progress



Flat or non-concentrating module prices have dropped as module efficiencies have increased. Prices are in 1985 dollars for large quantities of commercial products.



Typical module lifetimes were less than 1 year but are now estimated to be greater than 10 years. (Ten-year warranties are now available.)

Technology advancement in crystalline silicon solar cells and modules (non-concentrating).

Union Carbide Corporation (UCC) funded the now operational silicon refinement production plant with 1200 MT/year capacity. DOE/FSA-sponsored efforts were prominent in the UCC process research and development.

The automated machine interconnects solar cells and places them for module assembly. The second-generation machine made by Kulicke and Soffa was cost shared by Westinghouse Corporation and DOE/FSA

A Block I module (fabricated in 1975), held in front of four Block V modules, represents the progress of an 11-year effort. The modules, designed and manufactured by industry to FSA specifications and evaluated by FSA, rapidly evolved during the series of module purchases by DOE/FSA.

More technology advancements of the cooperative industry/university/ DOE/FSA efforts are shown on the inside back cover. Use of modules in photovoltaic power systems are shown on the outside back cover.

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Electricity from Photovoltaic Solar Cells

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Volume V: Process Development

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11 Years of Progress

October 1986

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Final Report Organization

This FSA Final Report (JPL Publication 86-31, 5101-289, DOE/JPL 1012-125, October 1986) is composed of eight volumes, consisting of an Executive Summary and seven technology reports:

Volume I: Executive Summary.

Volume II: Silicon Material.

Volume III: Silicon Sheet: Wafers and Ribbons

Volume IV: High-Efficiency Solar Cells.

Volume V: Process Development.

Volume VI: Engineering Sciences and Reliability.

Volume VII: Module Encapsulation.

Volume VIII: Project Analysis and Integration.

Two supplemental reports included in the final report package are:

FSA Project: 10 Years of Progress, JPL Document 400-279, 5101-279, October 1985.

Summary of FSA Project Documentation: Abstracts of Published Documents, 1975 to 1986, JPL Publication 82-79 (Revision 1), 5101-221, DOE/JPL-1012-76, September 1986.

Upon request, this FSA Final Report (JPL Publication 86-31) and the two supplemental reports (JPL Document 400-279 and JPL Publication 82-79) are individually available in print from:

National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Abstract

The Flat-Plate Solar Array (FSA) Project, funded by the U.S. Government and managed by the Jet Propulsion Laboratory, was formed in 1975 to develop the module/array technology needed to attain widespread terrestrial use of photovoltaics by 1985. To accomplish this, the FSA Project established and managed an Industry, University, and Federal Government Team to perform the needed research and development.

The goal of the Process Development Area, as part of the FSA Project, was to develop and demonstrate solar cell fabrication and module assembly process technologies required to meet the cost, lifetime, production capacity, and performance goals of the FSA Project. Early in the Assessment Phase, it became apparent that available processes were incapable of meeting the cost goals of the Project. Also, neither the 20-year (later increased to 30-year) reliability goal nor the effects of processing on reliability had ever been assessed.

This document is a summary of the FSA-sponsored research and development efforts expended by Government, Industry, and Universities in developing processes capable of meeting the Project's goals during volume production conditions. The cost goals allocated for processing were demonstrated by small volume quantities that were extrapolated by cost analyses to large-volume production. Program redirection precluded planned large-volume demonstrations and, in the final phase of the Project, efforts were directed toward research-oriented processing to produce high-efficiency cells. High-efficiency crystalline silicon solar cells are continuing to evolve in research laboratories. When efficiency increases resulting from these new cell designs level off, there is a need to develop high-volume, low-cost processes that will retain these efficiency improvements and capture the economic benefits.

To provide proper focus and coverage of the Process Development effort, four separate technology sections are discussed in this document: surface preparation, junction formation, metallization, and module assembly.

Foreword

Throughout U.S. history, the Nation's main source of energy has changed from wood to coal to petroleum. It is inevitable that changes will continue as fossil fuels are depleted. Within a lifetime, it is expected that most U.S. energy will come from a variety of sources, including renewable energy sources, instead of from a single type of fuel. More than 30% of the energy consumed in the United States is used for the generation of electricity. The consumption of electricity is increasing at a faster rate than the use of other energy forms and this trend is expected to continue.

Photovoltaics, a promising way to generate electricity, is expected to provide significant amounts of power in years to come. It uses solar cells to generate electricity directly from sunlight, cleanly and reliably, without moving parts. Photovoltaic (PV) power systems are simple, flexible, modular, and adaptable to many different applications in an almost infinite number of sizes and in diverse environments. Although photovoltaics is a proven technology that is cost-effective for hundreds of small applications, it is not yet cost-effective for large-scale utility use in the United States. For widespread economical use, the cost of generating power with photovoltaics must continue to be decreased by reducing the initial PV system cost, by increasing efficiency (reduction of land requirements), and by increasing the operational lifetime of the PV systems.

In the early 1970s, the pressures of the increasing demand for electrical power, combined with the uncertainty of fuel sources and ever-increasing prices for petroleum, led the U.S. Government to initiate a terrestrial PV research and development (R&D) project. The objective was to reduce the cost of manufacturing solar cells and modules. This effort, assigned to the Jet Propulsion Laboratory, evolved from more than a decade-and-a-half of spacecraft PV power-system experience and from recommendations of a conference on Solar Photovoltaic Energy held in 1973 at Cherry Hill, New Jersey.

This Project, originally called the Low-Cost Solar Array Project, but later known as the Flat-Plate Solar Array (FSA) Project, was based upon crystalline-silicon technology as developed for the space program. During the 1960s and 1970s, it had been demonstrated that photovoltaics was a dependable electrical power source for spacecraft. In this time interval, solar-cell quality and performance improved while the costs decreased. However, in 1975 the costs were still much too high for widespread use on Earth. It was necessary to reduce the manufacturing costs of solar cells by a factor of approximately 100 if they were to be a practical, widely used terrestrial power source.

The FSA Project was initiated to meet specific cost, efficiency, production capacity, and lifetime goals by R&D in all phases of flat-plate module (non-concentrating) technology, from solar-cell silicon material purification through verification of module reliability and performance.

The FSA Project was phased out at the end of September 1986.

Acknowledgments

Authorities in the field were used throughout this program as consultants to provide critiques, participate in critical technology reviews, and address specific technical problems. J. Parker, of Electrink Inc., and R. Vest, Director of the Turner Laboratory at Purdue University, were consultants in the area of material science; M. Wolf, of the University of Pennsylvania, consulted in the area of modeling and economics of specific processes; K. Wang, of the University of California, Los Angeles, consulted in the area of device physics; and Theodore Barry and Associates in production management.

Jet Propulsion Laboratory staff members were involved in laboratory research, technology critiques, process and problem analyses, and the technical management of contracts. The following engineers contributed to this program: D. Bickler (Area Manager), P. Alexander, D. Burger, J. Behm, D. Boyd, D. Fitzgerald, B. Gallagher, W. Hasbach, R. Josephs, A. Lawson, L. Sanchez, E. Drouet, C. Olson, and C. Radics. The contributions of support personnel, which included E. Fortier, L. Gee, K. Gray, L. Midling, J. Knox, and J. Stebbins, are gratefully acknowledged.

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FSA Project Summary

The Flat-Plate Solar Array (FSA) Project, a Government-sponsored photovoltaic (PV) project, was initiated in January 1975 with the intent to stimulate the development of PV systems for economically competitive, large-scale terrestrial use. The Project's goal was to develop, by 1985, the technology needed to produce PV modules with 10% energy conversion efficiency, a 20-year lifetime, and a selling price of $\$0.50/W_p$ (in 1975 dollars). The key achievement needed was cost reduction in the manufacture of solar cells and modules.

As manager, the Jet Propulsion Laboratory organized the Project to meet the stated goals through research and development (R&D) in all phases of flat-plate module technology, ranging from silicon-material refinement through verification of module reliability and performance. The Project sponsored parallel technology efforts with periodic progress reviews. Module manufacturing cost analyses were developed that permitted cost-goal allocations to be made for each technology. Economic analyses, performed periodically, permitted assessment of each technical option's potential for meeting the Project goal and of the Project's progress toward the National goal. Only the most promising options were continued. Most funds were used to sponsor R&D in private organizations and universities, and led to an effective Federal Government-University-Industry Team that cooperated to achieve rapid advancement in PV technology.

Excellent technical progress led to a growing participation by the private sector. By 1981, effective energy conservation, a leveling of energy prices, and decreased Government emphasis had altered the economic perspective for photovoltaics. The U.S. Department of Energy's (DOE's) National Photovoltaics Program was redirected to longer-range research efforts that the private sector avoided because of higher risk and longer payoff time. Thus, FSA concentrated its efforts on overcoming specific critical technological barriers to high efficiency, long life, reliability, and low-cost manufacturing.

To be competitive for use in utility central-station generation plants in the 1990s, it is estimated that the price of PV-generated power will need to be $0.17/kWh (1985 dollars). This price is the basis for a DOE Five-Year Photovoltaics Research Plan involving both increased cell efficiency and module lifetime. Area-related costs for PV utility plants are significant enough that flat-plate module efficiencies must be raised to between 13 and 17%, and module life extended to 30 years. Crystalline silicon, research solar cells (non-concentrating) have been fabricated with more than 20% efficiency. A full-size experimental 15% efficient module also has been fabricated. It is calculated that a multimegawatt PV power plant using large-volume production modules that incorporate the latest crystalline silicon technology could produce power for about $0.27/kWh (1985 dollars). It is believed that $0.17/kWh (1985 dollars) is achievable, but only with a renewed and dedicated effort.

Government-sponsored efforts, plus private investments, have resulted in a small, but growing terrestrial PV industry with economically competitive products for stand-alone PV power systems. A few megawatt-sized, utility-connected, PV installations, made possible by Government sponsorship and tax incentives, have demonstrated the technical feasibility and excellent reliability of large, multimegawatt PV power-generation plants using crystalline silicon solar cells.

Major FSA Project Accomplishments

- Established basic technologies for all aspects of the manufacture of nonconcentrating, crystalline-silicon PV modules and arrays for terrestrial use. Module durability also has been evaluated. These resulted in:
  - Reducing PV module prices by a factor of 15 from $\$75/W_p$ (1985 dollars) to $\$5/W_p$ (1985 dollars).
  - Increasing module efficiencies from 5 to 6% in 1975 to more than 15% in 1985.
  - Stimulating industry to establish 10-year warranties on production modules. There were no warranties in 1975.
  - Establishing a new, low-cost high-purity silicon feedstock-material refinement process.
  - Establishing knowledge and capabilities for PV module/array engineering/design and evaluation.
  - Establishing long-life PV module encapsulation systems.
  - Devising manufacturing and life-cycle cost economic analyses.
- Transferred technologies to the private sector by interactive activities in research, development, and field demonstrations. These included 256 R&D contracts, comprehensive module development and evaluation efforts, 26 Project Integration Meetings, 10 research forums, presentations at hundreds of technical meetings, and advisory efforts to industry on specific technical problems.
- Stimulated the establishment of a viable commercial PV industry in the United States.

Process Development Summary

The Process Development Area of the Flat-Plate Solar Array Project was initiated with the following goals: develop low-cost solar cell and module processes, design facilities and equipment to perform the processes, demonstrate fabrication in a pilot line, and transfer technology to industry. The terrestrial photovoltaics program was changed in 1981 to emphasize high-efficiency cell research. Facility and equipment design were curtailed and pilot line contracts redirected toward research. Research efforts were increased on the effects of processing on cell performance and in development of new processes in support of high-efficiency cell designs.

Accomplishments of 11 years of activity, in which more than 75 contracts were let, are grouped into two categories: low-cost processes and high-efficiency cell process research. These accomplishments are briefly mentioned below in each of four major technology areas: surface preparation, junction formation, metallization, and assembly:

- Surface preparation accomplishments related to low-cost cell fabrication were:
  - Development of alkaline etches for damage removal and texturizing.
  - Automation studies for reduced labor input.
  - Meniscus coating technology for pinhole-free films.
  - Screen-printed coatings for metal patterning.

  High-efficiency cell surface preparation process research showed:
  - Plasma processes are clean, but too slow.
  - Two-layer antireflective coatings are feasible and desirable.
  - Maintenance of surface cleanliness during processing is important for high efficiency.
- Junction formation accomplishments for low costs were:
  - Simultaneous front and back junction formation using liquid dopants.
  - High-rate ion implantation.
  - Non-mass-analyzed ion implantation.

  High-efficiency cell efforts resulted in:
  - Laser annealing using both solid-state and excimer laser technology.
  - Pulsed electron beam annealing.
  - Rapid thermal pulse annealing.
- Metallization processing was a special interest area because of its cost and reliability impact. Low-cost processing accomplishments were:
  - Thick-film, screenable ink printing with silver, aluminum, aluminum-silver, and copper.
  - Metallo-organic decomposition (MOD).
  - Silver-bismuth ink and liquid applications.
  - Reliable plating systems using palladium, nickel, and copper.
  - Initial high-efficiency cell processes in the area of laser pyrolytic decomposition of MOD films and producing reliable diffusion barrier films.
- Module assembly processes aimed at low-cost fabrication are directly transferrable to high-efficiency modules. Key accomplishments were:
  - Fully automated interconnection by soldering or by ultrasonic bonding.
  - Demonstration of robotic module assembly.
  - In-line ultrasonic cleaning.
  - Demonstration of automated module lay-up equipment.
  - Development of lamination process and equipment.
  - Demonstration of robotic terminal assembly and inspection.

The need to reduce costs was met by development and demonstration of processes that met Project goals for costs. Many new processes and equipment were developed; some are now standards in the industry. Pilot line operation was not accomplished because of redirection. Transfer of technology to industry was achieved with more than 140 processes documented. In the future, when new higher-efficiency solar cell designs are developed, it is anticipated that some new processes and equipment will be required for low-cost production that retains the efficiency improvements.

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SECTION I

Introduction

In 1975, the processes for fabricating solar cells for use on Earth were either those used for making space solar-cells or their derivatives. These techniques, borrowed from diode production technology, were very labor and material intensive with respect to the total product price.

The performance of individual solar cells was not consistent. Fabricated in batches, even the performances of those cells for use in space varied significantly. The best of these small rectangular "space cells" were assembled on panels, as closely packed as possible, to produce the maximum power per unit area. The lower performance cells were not used in spacecraft power systems because of high-performance requirements. Instead, these reject space cells were used for terrestrial applications. By that time, solar cells made specifically for terrestrial use had become competitive with reject space cells. These circular cells were made from one complete Czochralski (Cz) wafer. The cell processing was similar, but simpler and less expensive. For example, semiconductor industry-reject wafers were used. The result was that terrestrial solar-cell performance was less than space-cell performance. The challenge in 1975 was to reduce the cost of terrestrial solar cells, but still retain good quality and performance. The terrestrial solar cell evolved from the activities of the Flat-Plate Solar Array (FSA) Project, and differs appreciably (from a low-cost processing viewpoint) from the space solar cell.

The activities of solar cell processing and module assembly, as described in this document, are separated into four technology sections: surface preparation, junction formation, metallization, and module assembly.

A. OBJECTIVES

The basic objectives were to develop cell fabrication and module assembly process technologies required to meet cost and performance requirements for terrestrial photovoltaic (PV) power production. These process technologies were to be developed primarily by the private sector and managed by the FSA Process Development Area.

B. GOALS

The goals were to:

(1) Identify and develop low-cost cell and module production processes.

(2) Design facilities and equipment to perform the processes.

(3) Demonstrate fabrication of low-cost PV cells and modules in a pilot-line environment.

(4) Implement the transfer of mass production technology to industry.

C. IMPLEMENTATION PLAN

The Process Development Area formulated a plan to meet its area goals. The plan consisted of five phases that were compatible with the other FSA Project activities. The plan consisted of:

(1) Phase I, Technology Assessment: Determine availability and applicability of state-of-the-art cell and module processes.

(2) Phase II, Process Development: Develop applicable new processes.

(3) Phase III, Facility and Equipment Design: Develop automated equipment and facility designs for solar cell and module fabrication.

(4) Phase IV, Experimental Plant Construction: Incorporate previous efforts into a pilot line to define yields and determine remaining key cost factors.

(5) Phase V, Conversion to Mass Production: Transfer technology to industry.

The first three of the five phases covered the time span from 1975 through 1981 and were essentially completed. The fourth phase, Experimental Plant Construction, begun in 1980, was terminated in 1981 because of Project redirection. This redirection emphasized research-oriented efforts, leaving production and equipment concerns to the private sector. The fifth phase, Conversion to Mass Production, was deleted from the Project's plans and was left to the private sector for implementation. The completed phases are described below.

1. Phase I: Technology Assessment

Three Technology Assessment contracts were competitively awarded in early 1976, one each to Motorola, RCA, and Texas Instruments. Identification of those processes with the best potential for cost-effective implementation were selected, and recommendations for further study of those processes were made. More than 50 processes covering all areas of cell fabrication and module assembly were studied. Processes evolved that clearly distinguished terrestrial cells from space cells. As an example, copper metallization was identified as being more cost effective for top and bottom electrical conductors than either solder or silver. Metallization methods were expanded from space-oriented vacuum evaporation to include electroless plating, electrolytic plating, thick-film metal (printing), and reflow solder. Wafer surface treatments were expanded to include brushing, plasma etching, texture

etching, and new cleaning solutions. Junction formation, in addition to the standard space cell process (gaseous diffusion), was expanded to include spin-on and spray-on of liquid dopants, solid dopant diffusion, doped oxides, ion implantation, and advanced ion implantation. Other candidate cell processes that were added included silicon nitride chemical vapor deposition (CVD), oxide growths, mechanical edge grinding, and laser scribing. Assembly methods included the use of glass substrates, glass superstrates, and conductive adhesives, new encapsulation materials such as improved silicones, polyvinyl butyral (PVB), and ethylene vinyl acetate (EVA), and new cell interconnection methods. Selective processes were studied regarding their "sensitivity to variables" such as purity of input materials and supplies, and processing parameter variations such as time and temperature. Efforts at the Jet Propulsion Laboratory (JPL) were concentrated on process definition, sequence synergisms, and cell metallization analysis programs.

a. *Economic Analyses.* The problem facing the Project rather early in its inception was how to compare the potential production costs of competing processes and process sequences being investigated by various researchers. This was clearly evident during the Technology Assessment phase in which cost comparisons among the contractors investigating the same processes were significantly different. This pinpointed a need for a standard methodology that allowed relative comparisons between projected production costs attributable to competing processes.

Three key costing analysis tools were developed by Project Analysis and Integration (PA&I) personnel assisted by the Process Development Area. These tools were:

(1) Interim Price Estimation Guidelines (IPEG): A costing system simple enough to be run on a hand calculator. This method uses standard coefficients for costing inputs such as equipment, direct labor, material, floor space, and utilities.

(2) Solar Array Manufacturing Industry Simulation (SAMIS): A factory simulation that runs on a main frame computer. It has now been modified for use on a personal computer. This document requires the filling out of detailed costing sheets called Format A's used by the simulation program and model to produce process costs.

(3) Solar Array Manufacturing Industry Cost Standards (SAMICS): A catalog of material costs, labor cost, and other input costs that assisted the contractors in inputting standard costs.

These three techniques were verified and upgraded continually and used extensively throughout the life of the Project. In fact, items (1) and (2), above, are now available for use on an IBM PC and AT, respectively.

b. *Conclusions of Assessment Phase.* At the conclusion of the Assessment effort, it was determined that some existing processes were cost-effective, other processes and equipment required modifications, and that new processes and equipment were needed. The commonality among these processes was that they should: (1) result in improved efficiency, (2) consume a minimum of material and supplied, (3) use low-cost, recyclable supplies, and (4) have high production yields.

Before completing the assessment effort, automation and capital equipment were thought to be the major cost factors. It was shown that when labor is a significant cost factor in a process, the process should be automated. Most semiconductor processes were, to a significant extent, already automated. and, generally, capital costs for equipment could be distributed over large production runs resulting in low costs per unit.

2. Phase II: Process Development

The Technology Assessment phase had identified processes that the Process Development Area considered worthy of further development and study. Accordingly, Requests for Proposals (RFPs) for process development were distributed to the entire PV industry and were broadly scoped to include new and novel processes in addition to those processes identified in the Technology Assessment phase as requiring further development. Twenty PV industry contractors and two universities participated in this effort.

a. *Process Sequences.* An important part of the Phase II Development effort was the development of process sequences. Selection of an individual process depends upon what other processes are used before and after that process. Accordingly, the development of process sequences was initiated as a part of the Process Development effort. Discrete process steps were combined to form process sequences that were technically sound and cost effective. Contracts were either modified or awarded to develop and demonstrate viable, cost-effective sequences incorporating some of the discrete processes being developed. It became clear that there was no one single process sequence that was most cost-effective but that, rather, several process sequences could be demonstrated to be viable and cost-effective.

Collectively, the process sequences also showed the results of the cross-fertilization of technology that the FSA Project emphasized. The sequences illustrated the large number of possible low-cost process combinations that could be used to make a cell. The process sequences demonstrated that there was a new breed of solar cell whose fabrication processes were distinctly different from the space cell processes from which they evolved.

b. *Costing.* All contracts during the Phase II Process Development required: (1) process cost evaluations to be made using the costing methodology described above, and (2) the writing of process specifications. The cost documentation included all of the direct inputs for equipment cost and performance: required labor, floor space, utilities, maintenance, supplies, and input materials for each process.

c. *Process Specifications.* The process specifications were documents that described in detail all of the requirements needed to implement a process. These included input materials and chemicals; process parameters such as temperature, pressure, etc.; process equipment such as furnaces, evaporators, etc.; equipment power requirements; and all other facility requirements. The process specifications were a major tool used to transfer the evolving process technology to the entire PV industry. To obtain cross-fertilization, the distribution of process specifications was encouraged among PV contractors to verify processes. Near the end of the Process Development phase, more than 140 process specifications covering cell and module fabrication had been documented and distributed to interested PV industry members. Feedback on these requests showed industry verification of more than 40 of these processes.

d. *JPL Process Research Laboratory.* A Process Research Laboratory was created at JPL during the time of the Phase II Process Development activities. The purpose of the laboratory was twofold: (1) to verify the many processes being generated by the PV industry, and (2) to conduct independent process research.

3. Phase III: Facility and Equipment Design

Phase III, Facility and Equipment Design, began around mid-1979. This phase was accelerated in late 1979 by a bill sponsored by Senator Tsongas of Massachusetts. This bill provided additional funds to the U.S. Department of Energy (DOE) for near-term reduction of solar energy costs. Cost reduction ideas were solicited from industry through the JPL RFP system. Contracts were subsequently awarded and included the following:

(1) ARCO Solar: automated cell interconnection (solder based).

(2) Kulicke & Soffa: automated cell interconnection (ultrasonic weld based).

(3) Motorola: wax patterning; thin-cell processing.

(4) Photowatt: polysilicon cell processing; surface texturizing.

(5) RCA: megasonic cleaning.

In addition to the special near-term funding, the development of other process equipment was funded. Important process equipment developments were ion-implantation equipment, as mentioned earlier, for large-area junction formation and a pulsed electron beam annealing (PEBA) unit by Spire Corp., and a robotic cell interconnection and module assembly system by Tracor MBAssociates. The robotic equipment was especially meaningful because it demonstrated that cells could be handled robotically in large-volume quantities without breakage. These machines demonstrated the potential for high-volume production. The Facilities and Equipment Design phase (Phase III) was never heavily stressed because most of this technology was already being developed for the non-PV semiconductor devices.

4. Phase IV: Experimental Plant Construction

In late 1980, two Module Experimental Process System Development Unit (MEPSDU) contracts were awarded to provide the first controlled pilot-line data on cell and module processing. They were to be the culmination of the technology developed in the earlier phases. Prior to this time, the contractors produced cells and modules in a laboratory environment and then extrapolated the data for input into the SAMIS factory simulation program. In the MEPSDU contracts, each of the two contractors was required to construct and operate a pilot line. The contractors were required to record the production rate, yield, and process parameters. Three technical demonstration runs were required, two of which allowed no major adjustments, modifications, or repairs during and between runs. Solarex, Inc., and Westinghouse were competitively selected for the MEPSDU contracts. The two contractors chose diametric approaches. The Solarex process sequence would produce lower efficiency cells using low-cost processes. The Westinghouse process sequence would produce higher efficiency cells using more expensive processes. The Solarex process sequence used semi-crystalline silicon wafers, whereas the Westinghouse process sequence used dendritic web silicon. Ultrasonic bonding of cell interconnections to the solar cells was to be used by Westinghouse, and soldered cell interconnections were to be used by Solarex. Vacuum lamination was the proposed module assembly technique for both process sequences.

D. PROJECT REDIRECTION

By mid-1981, the budget of the FSA Project had been reduced to an extent that a major redirection toward research-oriented efforts was made which affected every area activity of the FSA Project. The Phase IV MEPSDU effort was cancelled and Phase V, Mass Production (which was never started), was also cancelled.

The Process Development Area redirected efforts toward basic process research and, later, toward higher-efficiency cell process research.

The Westinghouse MEPSDU effort was redirected to investigate liquid-dopant processing for junction formation, which ultimately replaced the gaseous diffusion process on the Westinghouse pilot line. The Solarex MEPSDU effort was redirected toward investigating process mechanisms affecting lifetime and performance of cells made from polycrystalline material.

A Cell Metallization Research Forum was held in 1983 which clarified and defined the state of the art of current solar-cell metallization systems. This Forum opened up a number of new technology areas, some of which were later explored under development contracts.

Process control became a major area of concern as industry yields were not as high nor as predictable as had been expected. Industry proprietary concerns and lack of large-scale engineering pilot lines limited the availability of data. To overcome the lack of information

and to explore processing for higher-efficiency cells, process and device modeling capabilities were investigated. A device model called SPCOLAY, developed by the University of Pennsylvania, was exercised by the Process Development Area and found to be especially useful in defining the interactions between cell substrate material parameters and preferred cell processes.

The term "directed energy research" was coined to describe the increased emphasis on high-efficiency processes, which covers the use of microwave, laser, and thermal pulse energy sources. All of these new energy sources were of technical interest because they allow many cell processes to be performed without heating the bulk of the substrate. PV cell fabrication by "cold" processing is used to avoid degradation of bulk substrate properties, specifically minority carrier lifetime.

Results from directed energy research contracts were gratifying. Westinghouse demonstrated that thermal pulse (heat lamps) can be used to simultaneously form n and p^+ junctions using liquid dopants. Previous processing required more handling, cleaning, and the use of expensive oxide masks. Excimer lasers were scaled up and were used by ARCO Solar and Spire for annealing ion-implanted junctions. Superwave Technology developed a microwave-powered plasma system for thin-film silicon nitride deposition. Argon lasers were used by Westinghouse in a successful metallization method in which the laser scanned wafers covered with metal, bonding the metal to the solar cell where the "laser writing" had occurred, thereby eliminating the costly photolithography process.

The research-oriented efforts also led to development of metallo-organic decomposition (MOD) inks by Purdue University. The MOD ink process uses liquid compounds containing metal atoms attached to organic compound structures such as neodecanoic acid. When these liquid compounds (inks) are coated on cells and heat is applied, the compound decomposes giving off gases and leaving a deposited metal on the cell surface. One of the MOD inks, silver neodecanoate, was successfully demonstrated on the Westinghouse laser-writing metallization contract. The MOD inks were also demonstrated in the development of an Ink-Jet Printer system at Purdue University. In this application, the MOD ink was deposited onto cells by means of an Ink-Jet Printer which ejected the MOD ink through nozzles onto the cell in a configured pattern.

E. SUMMARY COMMENTS

The research-oriented thrusts during the last period of the FSA Project culminated an 11-year effort. In the Process Development Area, processing technologies were identified and developed that clearly distinguished terrestrial cell processing from space cell processing by the use of new or less sophisticated processes requiring fewer manufacturing steps. Objectives and goals were met within the constraints of budgetary funding levels. During the 11-year Project life, more than 75 contracts were awarded by the Process Development Area.*

The basic elements of cell processing (which are defined as surface preparation, junction formation, metallization, and module assembly) are described in detail in this report and reflect the depth and diversity of effort that was expended in these process elements.

*A list of these contracts is contained in a supplemental report included in the final report package: *Summary of Flat-Plate Solar Array Project Documentation: Abstracts of Documents, 1975 to 1986*, JPL Publication 82-79, Revision 1, JPL Document 5101-221, dated September 1986.

SECTION II

Surface Preparation

A. BACKGROUND

Processes considered in this surface preparation section are: damage etching, texturizing, prediffusion cleaning, plasma etching, antireflective (AR) coating of cells, metal patterning, and scrubbing.

Surface preparation processes have historically been very important, but have achieved little attention or acclaim. This was the case in 1975 when most of the semiconductor and PV industries were using wet chemical cleaning and etching processes.

The demand for low-cost processing of PV devices required development of processes different from those used in semiconductor fabrication. Progress in these diverse efforts is detailed below in rough chronological order. First, however, the technical requirements for success must be defined by looking at the theory.

B. THEORY

All of the surface preparation processes have some chemical or physical theoretical basis. However, only two processes require discussion of the theory to understand the development efforts. Texturizing and AR coating will be discussed below.

1. Texturizing

The texturizing process makes use of chemistry and crystallography to form an efficient light absorbing surface on a silicon wafer (Figure 1). Most PV cells are made from Cz-grown single-crystal silicon wafers with a (100) orientation. This orientation has two crystallographic planes intersecting the wafer surface at an angle of 54.7 deg and at right angles to each other. When these crystallographic planes are exposed to an anisotropic etchant, there is a preferential removal of material resulting in the formation of square pyramids as shown in Figure 1.

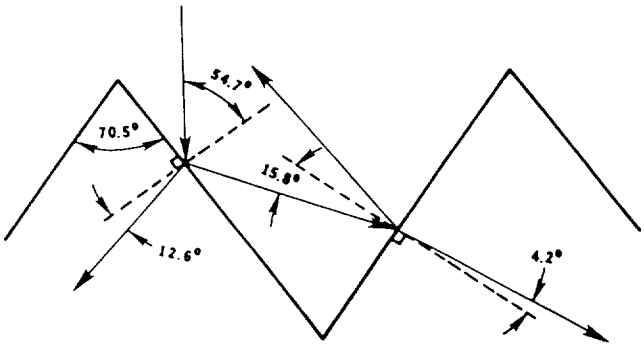


Figure 1. Reflected and Refracted Ray Traces and Angular Relations for Light Normally Incident to the Substrate (100) Plane of a Textured Surface Solar Cell

Light striking the side of a pyramid is partially absorbed and partially reflected. The reflected portion of the light then strikes another pyramidal face and is mostly absorbed because its incident angle is more nearly perpendicular.

2. Antireflective Coating

An AR coating is used to reduce the amount of sunlight reflected (and, thus, not collected) from the surface of a bare PV cell. Reflection and transmission of electromagnetic radiation (this includes light) at the boundary between two materials with different refractive indices can be determined by solving Maxwell's equations with the appropriate boundary conditions (Reference 1).

For non-absorbing media (true of silicon for short distances), the resulting equations are:

$$R = |r_{01}|^2 \text{ and } T = \frac{\eta_1 \cos \phi_1}{\eta_0 \cos \phi_0} |t_1|^2$$

where

R = reflectance

T = transmittance

r_{01} and t_1 = Fresnel coefficients which are functions of the refractive indices η_0 and η_1 of the two media and the angles ϕ_0 and ϕ_1, which the incident and transmitted waves make with the surface normal, respectively

For a single surface:

$$r_{01} = \frac{\eta_0 \cos \phi_0 - \eta_1 \cos \phi_1}{\eta_0 \cos \phi_0 + \eta_1 \cos \phi_1}$$

If the first medium is air and the second is silicon, then $\eta_0 = 1$ and $\eta_1 = 3.85$ (assuming a λ of 550 nm). If normal incidence is assumed, then the amount of reflected light is:

$$R = |r_{01}|^2 = \left(\frac{\eta_0 - \eta_1}{\eta_0 + \eta_1}\right)^2 = \left(\frac{2.85^{\ 2}}{4.85}\right)$$

$$= 0.345$$

If a thin layer of a material with a refractive index between that of air and silicon is added to the surface, the equations become more complex. Briefly, if a thickness equal to an odd number of quarter wavelengths of light is added, then a destructive interference of reflected waves is established. This condition produces the least reflectance. Because transmittance decreases as film

thickness increases (because of absorption), the usual AR coating thickness is 1/4 wavelength.

For normal incident light, the reflectance of a single AR coating of optimum thickness would be found from the following equation:

$$R = \left(\frac{\eta_1 \eta_3 - \eta_2^2}{\eta_1 \eta_3 + \eta_2^2} \right)^2$$

If the index of refraction of the AR coating is 1.96 (silicon nitride), then the reflectance is:

$$R = \left(\frac{1.0 \times 3.85 - (1.96)^2}{1.0 \times 3.85 + (1.96)^2} \right)$$

$$= 0.001$$

However, this low reflectance is only true for one wavelength (550 nm) because the quarter wave condition for destructive interference is only true for one wavelength of light. Both silicon and silicon nitride have somewhat different refractive indices at different wavelengths. An additional consideration is that the cells are usually mounted behind a glass superstrate with a refractive index of 1.52. The optimum η of the AR coating is now 2.4.

The rather restrictive optimum wavelength condition can be changed by spreading the passband using multiple layers of AR coating or by using a graded layer with variable refractive index. In either case, additional films are more costly and provide diminishing returns. The optimum number of AR layers for PV cells is two or, at most, three depending upon the materials.

C. STATUS AS OF 1975

Surface preparation processes in 1975 were oriented toward terrestrial PV cells made using gaseous diffusion and electroless plated/solder dipped metallization. The remaining cell process steps were oriented toward preparing or modifying the silicon surface to enhance processing or cell performance. These processes are discussed briefly to provide a background for the discussion on process development.

1. Damage Removal and Texturizing

When a wafer is sawed from an ingot, the sawing process creates numerous surface microcracks. The cheapest way to remove this damaged layer is to etch at least 0.5 mil of silicon from both sides of the wafer using an isotropic etchant. The resulting surface is flat with a silvery-grey matte finish from small pits and other etching and sawing irregularities.

Texturizing is a controlled etching process using an etchant that is not isotropic. The etchant creates a rough surface with a dark grey finish from the 1- to 10-μm pyramids on the surface. Texturizing must be carefully done to ensure formation of pyramids in the right size range over the entire surface. Subsequent wafer handling must also be done with care because the texturized wafers are more fragile than polished or damage-etched wafers.

2. Cleaning

Cleaning just prior to junction formation is a very important process step. Any surface contaminants will degrade cell performance should they diffuse into the silicon and will affect the structure of the junction. Prediffusion cleaning also promotes process uniformity. An acid etchant system is usually used for prediffusion cleaning. Other specific cleaning processes are tailored to the major process being performed (e.g., prior to metallization).

3. Rinsing and Drying

These processes are often overlooked. Unless a contamination-free environment is maintained during rinsing and drying, the cleaning step will have been in vain. High purity deionized (DI) water is commonly used for rinsing. Maintenance of DI water purity is not simple, and semiconductor production lines have been shut down because of chemical or biological contamination of the process water system.

4. Metal Patterning

Creating a fine grid line pattern of metal on a PV cell can be achieved in a variety of ways. The simplest patterning process is a shadow mask. A metal mask is held over the surface of a wafer during evaporative deposition of metal in a vacuum. The deposited metal passes through openings in the mask. Another patterning method is the use of photolithography. A photosensitive resist is applied to the wafer surface and the desired metal pattern is imprinted on the resist using a high-intensity light and photomask. The photoresist is then removed from the area to be metallized by use of a developer. An evaporated metal coating is then selectively removed by solvent liftoff.

Another patterning method is to print an acid resistant mask on the wafer surface and subsequently apply metal using an electroless plating bath.

5. Antireflective Coating

An AR coating is usually applied to PV cells in either of two ways: polymer coating or CVD. The polymer coating material can be applied by spinning, dipping, spraying, or meniscus coating. After application, the polymer solvents and binders must be driven off by baking.

A CVD process requires the use of heat to decompose a gaseous precursor and deposit the desired material on a cell. Either low-pressure, atmospheric-pressure, or plasma-enhanced CVD processes can be used.

All of the above processes required expensive, contamination-free chemicals and many create undesirable effluents. Reduction of costs and effluents were early Process Development Area goals.

D. PROCESS DEVELOPMENT

The first cell processing cost studies showed that subtractive processes were wasteful and wet chemistry was expensive. The development of these findings and subsequent efforts to resolve them are detailed in chronological order below.

1. Phase I

The Assessment Phase of the Automated Array Assembly Task (now the Process Development Task) was a compilation and evaluation of available semiconductor and PV industry processes. Because the three major contractors in this phase (Texas Instruments, RCA, and Motorola) all came up with different approaches, results from this effort are discussed by process type.

a. *Damage Removal and Texturizing.* Only Motorola placed much emphasis on a damage removal etch. Their proposed process involved use of an ultrasonic tank to remove silicon chips and an alkaline (NaOH) etchant. RCA had a "Z clean" process using hot Caro's (1:1 H_2SO_4:H_2O_2) acid and a DI water cascade rinse. Both Motorola and Texas Instruments felt that texturizing was a viable, low-cost process. Texas Instruments investigated both an alkaline (NaOH) and a hydrazine etch with the alkaline etch favored because of cost and safety considerations.

A prediffusion clean or clean etch was part of all three final process sequences. Motorola used their texture etch for prediffusion cleaning. Texas Instruments discussed water-based (polar), organic solvent-based (nonpolar), and plasma-cleaning alternatives with no stated preference. Motorola had an acid etch clean and a plasma clean process that should be mentioned. Their process sequence was unusually long and well documented with 26 cell process steps. RCA used a three-step prediffusion clean: SC-1 (a 1:1:5 mixture of ammonia, hydrogen peroxide, and water), hydrofluoric acid, and SC-2 (a 1:1:5 mixture of hydrochloric acid, hydrogen peroxide, and water).

Rinsing was already mentioned as part of one acid cleaning step. The only mention of rinsing as a discrete process step was the use of a high-pressure scrubber by Motorola. Motorola was also the only contractor who mentioned drying. A large spin dryer or centrifuge was suggested for drying a large number of wafers economically.

Metal patterning, however, was discussed at great length by Texas Instruments and mentioned by the other two contractors. The pattern optimization analysis by Texas Instruments was the basis for subsequent computer optimization efforts at JPL. Selection of a specific metallization pattern is an interactive process. Process costs and capabilities must be balanced against cell power loss because of resistance and shadowing. Possible patterning methods are:

(1) Metal shadow mask.

(2) Screen-printed wax or acid resist.

(3) Photolithography and metal etch.

(4) Photolithography, dielectric (e.g., Si_3N_4) etch, and electroless plate.

(5) Photolithography and solvent liftoff.

(6) Dry film (© Du Pont) and metal etch.

(7) Mid-Film (© Ferro Corp.), metal powder, and sinter.

(8) Screen-printed thick-film ink.

(9) Direct write with laser.

An AR coating was considered a necessity by all three contractors. RCA favored a spray-on polymer coating mixture of SiO_2 and TiO_2 with a two-stage bake at 200 and 400°C. Motorola used a low temperature CVD deposition of Si_3N_4. Texas Instruments investigated both processes. The RCA report compared the SiO_2 + TiO_2 coating to an evaporatively deposited and thermally oxidized film of Ta_2O_5. Both coatings performed well. A major concern was control of coating thickness which should, theoretically, be held to within ±5% of the designed thickness.

Completion of the assessment phase resulted in a list of interesting and economically feasible processes. Not all of these processes were compatible with one another, with other potential cell processes, nor with the capital equipment capabilities of the PV industry. Additional development was needed.

2. Phase II

Development of various cell surface preparation processes often took place in conjunction with other process efforts. This association effect meant that few contracts were let for specific surface preparation processes. Because of this development history, it is difficult to group or otherwise characterize various contracts. Significant developments by various contractors are discussed in the following paragraphs.

Motorola found that a pre-plating cleaning was of special importance in their immersion palladium plating process (Reference 2). Immersion plating is an especially surface-sensitive process and, in the Motorola process sequence, it followed a photolithographic patterning of a silicon nitride AR coating. Photoresists used to be heavily contaminated with metals, so a contaminated surface was suspected. After some experiments, the final clean procedure was established as:

O_2 Plasma Clean

50:1 H_2O:HF Etch

DI H_2O Rinse

Aqua Regia Etch (3:1 $HC1:HNO_3$)

DI H_2O Rinse

50:1 H_2O:HF Rinse

Immersion Plating

Note the use of both plasma cleaning and chemical etches. Spin-dry and hydraulic high-pressure water spray scrubbing were also used as part of the overall metallization process sequence.

Throughout the process development effort, the University of Pennsylvania was on contract to provide analysis and evaluation. At JPL's request, the University of Pennsylvania prepared a report on metallization and patterning methods (Reference 3). The first 90 pages of this report are concerned with gridline design optimization. The final design rules (14 in number) cover two pages and are quite comprehensive. Patterning of the metallization is covered in each of four different metallization and patterning scenarios:

(1) Screen-printed thick-film silver.

(2) Vacuum deposited nickel (photoresist liftoff).

(3) Sputtering of copper (chemical etch).

(4) Electroless nickel (screen-printed resist) and solder dip.

This was a good conceptual report and it pointed out the need for continuing process development, yield improvement, and cost reduction.

Optical Coating Laboratory, Inc. (now Applied Solar Energy Co.), had a long history of producing space cells. During a module design contract, they applied a proprietary multilayer AR coating to maximize cell and module efficiency (Reference 4). This AR coating was optimized for use with a glass cover or superstrate. An additional heat rejection coating was also applied, but was not beneficial because of excessive light absorption.

A follow-on contract to Motorola led to more investigation of their Si_3N_4 AR coating and plasma cleaning processes (Reference 5). Silicon nitride can be used for four different purposes on a PV cell surface: AR coating, surface passivant, metallization pattern mask, and diffusion barrier. When the Si_3N_4 coating is etched from the silicon cell surface, it allows the immersion plating process to take place only on the exposed silicon surface. Although palladium (commonly used for immersion plating) is an expensive material, the overall cost saving was of interest. A metal masked plasma etch was successfully used to define a fine gridline structure in a Si_3N_4 coating even with a mask to substrate distance as great as 10 mils (Figure 2). After immersion, palladium, electroless nickel, and electrolytic copper layers were added. The Si_3N_4 was found to be an adequate diffusion barrier against copper. Plasma texturizing and damage removal were also studied and were shown to be technically feasible, but not cost effective.

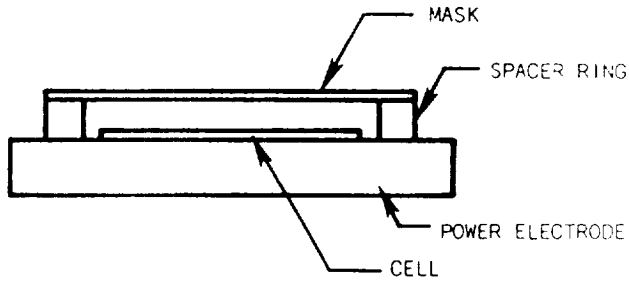


Figure 2. Etch Mask Configuration

Another plasma etching study was conducted by Westinghouse R&D Center on their dendritic web material (Reference 6). It was found that plasma etching did not remove the in situ oxide film found on freshly grown dendritic web. The Motorola metallization system was investigated, but the chemicals attacked the AR coating. Silicon nitride could not be used as a mask because of stresses that caused excessive web bowing. At Westinghouse, the AR coating was applied by dipping with a controlled web removal rate from precursors with standard compositions and viscosities.

MBAssociates, a non-PV industry company, looked at standard PV or semiconductor industry processes from the standpoint of automation and process verification (Reference 7). Among the processes studied were: damage etch, cascade rinse, texturize, and prediffusion cleaning. All of these steps were found to be feasible, economic, and easily automated. The prediffusion clean step showed that iron is a common contaminant in the sodium hydroxide etch and texturize baths. Iron could easily be removed by a soak in 3% sulfuric acid.

As part of the process verification and automation program, Lockheed Missiles & Space Co., Inc. also looked at some of the PV cell processes (Reference 8). The surface preparation steps that they studied were texture etch and spray-on AR coating. The Lockheed cost and automation design efforts were very detailed and have served as examples to the rest of the PV industry. The texture etch processing equipment is shown in Figure 3. During the study, it was found that a preliminary acid flash etch process could be dropped and the cells placed in the texturize process for damage etching. Spray-on AR coating was preferred for use with the rough, texturized cells.

A contract with Texas Instruments examined the feasibility of an inter-digitated back contact, tandem junction cell design (Reference 9). Grid lines are on the back in this cell design as shown in Figure 4. The processing cost and complexity were too great for the demonstrated efficiency increase, so this design option was not pursued in the Process Development Area.

A simplified, environmentally resistant process sequence was developed by Kinetic Coatings, Inc. (Reference 10). The four basic steps were: apply front and back contacts by sputtering; apply front coating of aluminum oxide to provide AR film, hermetic seal, and

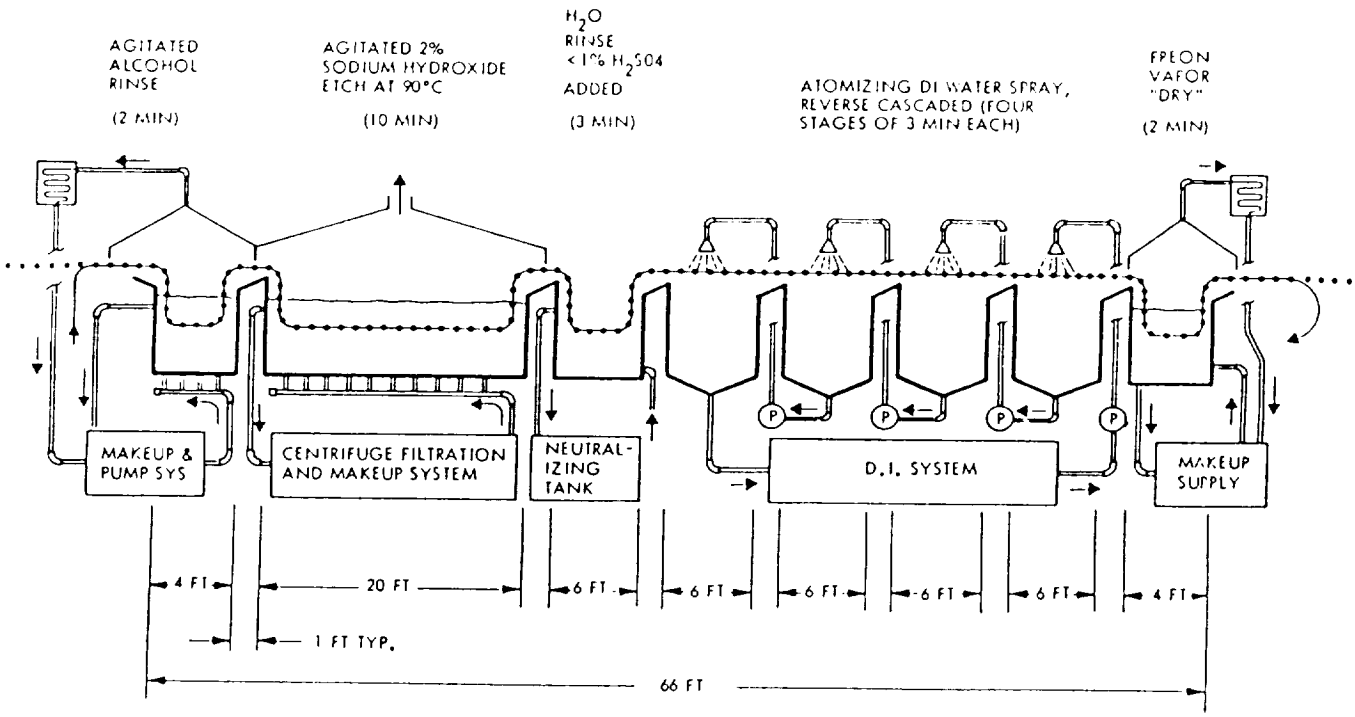


Figure 3. Texture Etch Process

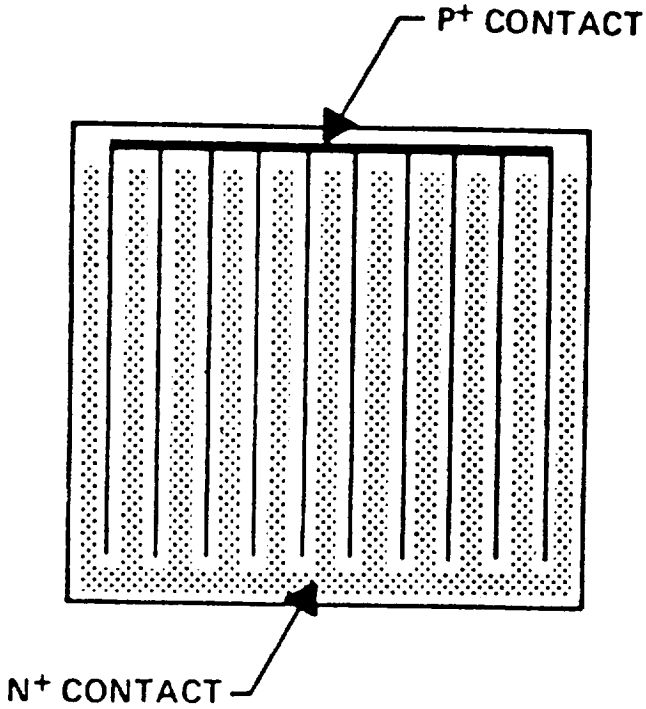


Figure 4. Metallization Pattern for Back of 2 × 2 cm Tandem Junction Cell

implantation oxide; ion implant front; and heat treat to activate implanted ions and alloy contacts. Although the aluminum oxide coating resulted in a highly absorptive surface, other processing problems prevented further development effort on this approach.

Optical Coating Laboratories, Inc., worked on grid line optimization and development of plating masks (Reference 11). A screen-printed resist was used to define a grid pattern in the SiO_2 AR coating. Subsequent metallization was electroless nickel and electrolytic copper. The grid lines that were produced created shadows over 10 to 12% of the cell top surface, which is a common problem with screen-printed patterns.

Polycrystalline silicon substrates were being developed; this raised some questions as to proper cell processing. Photowatt International, Inc., looked into the effects of grain size on efficiency, proper grid line design, and the texturize process (Reference 12). Grain boundary recombination was considered to be a serious problem and a series of grid line designs was investigated. The conclusion was that grain boundary degradation was not a grid design problem, but that large variations of results indicated some inherent material or processing problems. It was also found that polycrystalline silicon cells texturize at a slower rate than single crystal cells and have a different degree of texture dependent upon grain orientation. An optimized polycrystalline texturizing process was defined.

An inexpensive etch resist was desired, and this effort was pursued by Motorola (Reference 13). A wax-based resist was sought that could be printed onto the cell and later removed by hot water. Any solvent removal operations were considered to be environmentally undesirable. Problems with application, wax spreading, and removal prevented any feasible process development.

Removal of surface contaminants and particulates was a constant concern and RCA applied their semiconductor technology to find a solution (Reference 14). A continuous cleaning system was developed which used an ammonia-hydrogen peroxide solution and an ultrasonic tank. The solution is not an environmental hazard and can be recycled many times. A laser monitor was used to determine cleaning efficiency. A high-velocity air drying system was used at the end of the cleaning cycle to provide rapid, non-polluting wafer drying.

A special study for the Encapsulation Task of the FSA Project tabulated the effect of pottant and superstrate (cover glass) index of refraction on module efficiency (Reference 15). A total of 14 tables were calculated and show module efficiency coefficients for a number of different cell designs and cover glass/pottant combinations.

The Westinghouse Advanced Energy Systems Division had taken over the process development of dendritic cells and was examining some new process options (Reference 16). One approach to cell processing is to use a SiO_2 diffusion mask to cover one cell surface while the other is being diffused. This effort was successful, but was considered too costly. A new polymer film application method, meniscus coating (Figure 5), was tried with great success. A meniscus coater was successfully used to apply AR coatings, diffusion masks, and polymer dopants. The only problems encountered were with clogging or too rapid drying of film mixtures not originally intended for this type of application.

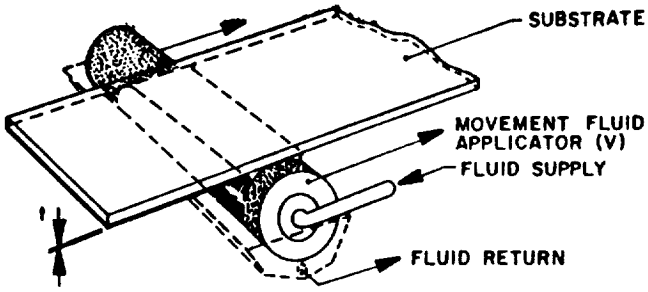


Figure 5. Meniscus Coater Liquid Application Device

Excimer laser annealing studies were profoundly affected by surface treatment according to ARCO Solar, Inc. (Reference 17). Chemical etching did not remove particulates which interfered with the annealing process. Any surface brushing or scrubbing also created problems. Another source of problems was the DI water rinse where filtration of submicron particulates was required.

It is interesting to note that all of these problems were created because of the change of one process step: laser annealing. The same laboratory that had the problems was successfully producing good PV cells with their standard processes.

E. RELIABILITY

Long-term module reliability is a function of cleanliness of components. Removal of undesirable contaminants had been one of the main concerns of the surface preparation contracts. There are other major reliability issues, but none seem likely to be affected by any of the other surface preparation processes.

F. ECONOMICS

Improvement of cell efficiency can be achieved most inexpensively by texturizing the cell. Many current PV industry manufacturers presently use a texturizing process. A double layer AR coating can also be an economical process, depending upon the deposition process selected and the product throughput. Because all of the surface preparation processes were lumped together with the remaining cell processes, it is difficult to put a value on any one specific cell process. In 1975, cell processing cost about $\$2.00/W_p$. Today, cell processing costs about $\$0.35/W_p$ after inflation. Allowing for inflation, the reduction in cell processing cost during the FSA Project was about a factor of 10. Automation, improved processes, and increased cell efficiency were all important parts of this cost reduction effort.

G. KEY ACCOMPLISHMENTS

Improvements in surface preparation processes have been discussed in detail above. A summary of the key accomplishments is listed below by process:

(1) Generic Process Developments

- (a) Automation studies proved technological and economic feasibility of automation.
- (b) Cell efficiencies are very dependent upon surface cleanliness.
- (c) Meniscus coating is an inexpensive and economical coating process.
- (d) Test patterns were developed and found to be very useful process development and monitoring tools.

(2) Damage Removal and Texturizing Processes

- (a) Damage removal by alkaline etch was developed and substituted for the more expensive acid etches.
- (b) Plasma etch processes were found to be too slow and, therefore, too expensive.
- (c) The texturizing process was developed and transferred to industry where it is now a standard process.
- (d) An optimized texturizing process for polycrystalline silicon cells was developed.

(3) Cleaning Processes

(a) Plasma cleaning was found to be uneconomical.

(b) High-pressure water spray is preferred to brush scrubbing or particulate removal.

(c) The Megasonic cleaning process was developed, transferred to industry, and is now a standard technique.

(4) Rinsing and Drying Processes

(a) High-velocity air is an economical drying process.

(b) Spin dry is a preferred drying process.

(5) Metal Patterning Processes

(a) Plasma patterning was shown to be feasible, but too costly.

(b) Screen printing is a low-cost approach, but limits cell efficiency because of excessive grid line width.

(6) Antireflective Coating Processes

(a) A heat rejection coating is a questionable benefit because of excessive light absorption.

(b) Silicon nitride is an excellent multipurpose cell coating.

H. CURRENT STATUS

The only work being done on surface preparation processes at present involves high-efficiency cell designs. Some of these designs use multiple layer AR coatings. However, present studies are not focused on surface preparation process development.

I. REQUIRED FUTURE TECHNICAL NEEDS

Future technical needs in surface preparation processes are contingent upon the results of research in the design of high-efficiency solar cell structures. Present research has been emphasizing passivating layers and AR coatings that use laboratory equipment which are not amenable to high-volume production. Future needs of surface preparation processes, such as these, will require development of production equipment.

SECTION III

Junction Formation

A. BACKGROUND

Junction formation technology was well established in 1975 when the FSA Project was formed. However, the terrestrial solar cell introduced new considerations in junction formation, especially with respect to the cost of fabricating solar cells in mass production. In addition to the standard gaseous diffusion process employed by the space cell industry, the terrestrial cell industry examined other junction-forming techniques such as: liquid dopants applied by spraying, spinning, or dipping; and large-volume ion implantation techniques followed by PEBA or excimer laser annealing; in addition to standard furnace annealing. New diffusion drive-in techniques such as rapid thermal processing (RTP) were examined. Printed metal (aluminum) back surface junctions were investigated and used. Even the standard gaseous-diffusion junction-forming processes were reexamined from a standpoint of equipment design to yield high volume throughput. This section deals with the efforts of the PV industry, under the Process Development Area management, to investigate the cost effectiveness, reliability, amenability to automation, and performance of different junction forming techniques.

B. THEORY

1. General

The theory of semiconductor behavior has been expanding and developing for nearly 40 years, going back to the invention of the transistor in 1947. The solar cell itself is just one of many types of semiconductor devices and goes back to the early 1950s when it was invented at Bell Laboratories. A solar cell differs from most semiconductor devices in that it is a power generating device, whereas most semiconductor devices consume electrical power to function. The p/n junction is the heart of this generating device.

An intrinsic (undoped) slice of silicon when exposed to the solar spectrum will absorb light. The photons will collide and exchange momentum with the electrons of the silicon atoms. As a result of these collisions, some of the silicon electrons will be boosted into the conduction band, leaving behind holes in the valence band. Figure 6 is a schematic showing electrons being boosted into the conduction band. If there are no additional impurities in the silicon slice, the free-moving electrons will simply recombine at the hole sites and the net effect of absorbing light would be to heat up the silicon slice.

However, if the lower part of the silicon slice were doped (in a controlled fashion) with a p-type impurity, such as boron, and if the upper portion of that slice were doped with an n-type impurity, such as phosphorus, then the silicon slice would behave in a different

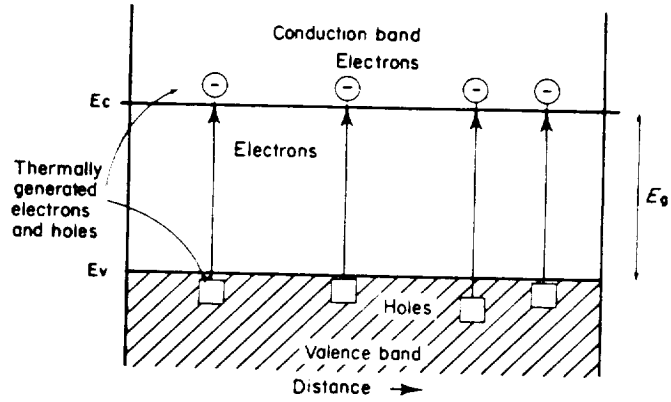


Figure 6. Simple Band Diagram of a Semiconductor

manner. The interface where the two types of impurities meet is called the n/p junction. If this doped silicon slice were now exposed to light, collisions of photons with the phosphorus-doped silicon atoms would produce an excess of electrons. This is because the phosphorus atoms have five electrons (valence electrons) in their outer shells which is one more electron than is needed for covalent bonding with the silicon atoms. Conversely, collisions of photons with the boron-doped silicon atoms would produce an excess of holes. This is because the boron atom lacks one electron to complete a covalent bond with the silicon atom. Figure 7 is a schematic concept of the generation of electrons and holes in n- and p-type silicon.

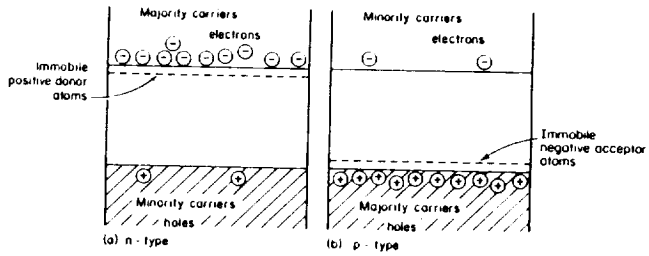


Figure 7. Simple Band Diagrams of (a) n-Type and (b) p-Type Silicon

The net effect of creating excess electrons and holes in the silicon slice is to produce an electric field with a polarity that accelerates electrons toward one surface and holes toward the other surface. When metal contacts are placed on the front and back surfaces of such a device and electrically connected through an electrical load, then current will flow. The physics of solar cells are adequately described in References 18 through 22.

Although one aspect of junctions involves the physics of how and why junctions work, covered very briefly above, a second aspect of junctions is how they are formed and the techniques used to form them. It is this second aspect of junctions (junction formation) that involved the Process Development Area.

2. Forming Junctions

a. *Gaseous Diffusion.* One of the commonly used techniques for forming junctions is to start with the host material already doped with an impurity and then to diffuse a second species of impurity into the host material. In solar cell fabrication, the starting host material, silicon, is doped in the melt with either boron or phosphorus to form p- or n-type silicon, respectively. The dopant that must be diffused to form an n/p junction with p-type silicon is normally a Type V compound that contains phosphorus or arsenic. Similarly, the dopant that must be diffused to form a p/n junction with n-type material is normally boron or one of the other Type III compounds. An $n/p/p^+$ solar cell structure, for example, would have a phosphorus-diffused front layer forming an n/p junction with p-type (boron-doped) silicon followed by an enhanced boron diffusion to form a back p/p^+ junction.

The basic diffusion procedures are: (1) introduce a dopant-containing compound such as BBr_3 or $POCl_3$ into a diffusion tube, (2) oxidize the compound and then reduce the dopant oxide by reaction with the silicon surface, and (3) the dopant is then thermally diffused to form a junction.

In the case of a p/n or p/p^+ junction formation, N_2 is bubbled through a BBr_3 solution and carries the entrained vapor into the diffusion tube. Oxygen is introduced separately:

(1) The oxidation reaction is:

$$4BBr_3 + 3O_2 \longrightarrow 2B_2O_3 + 6Br_2$$

(2) The reduction reaction (delivering boron to the silicon surface) is:

$$2B_2O_3 + 3Si \longrightarrow 4B + 3SiO_2$$

(3) The boron is then thermally diffused into the silicon surface.

Similarly, an example of an n/p junction formation would be where N_2 (a carrier gas) is bubbled through a $POCl_3$ solution and carries the entrained vapor into the diffusion tube. Oxygen is introduced separately.

(1) The oxidation reaction is:

$$4POCl_3 + 3O_2 \longrightarrow 2P_2O_5 + 6Cl_2$$

(2) The reduction reaction (delivering phosphorus to the silicon surface) is:

$$2P_2O_5 + 5Si \longrightarrow 4P + 5SiO_2$$

(3) The phosphorus is then thermally diffused (or driven) into the silicon surface.

The reactions above are highly idealized. In practice, the common assumption is that a dopant-rich glass is formed after the reduction reaction (a phosphosilicate or borosilicate glass, depending on the type of impurity). This glass (or film) becomes an inifinite source of the dopant. The distribution of the dopant (phosphorus or boron) into the silicon follows the complementary error function (erfc) distribution curve during the glass formation or deposition step of the diffusion process. The erfc is based upon distribution from an infinite source which the glass provides. The drive-in step [step (3), above], which occurs after the glass is formed, further distributes the impurity by a Gaussian distribution. The Gaussian distribution is based upon distribution from a finite source, which is assumed, after the deposition step has been completed. For shallow junctions of less than 0.5 μm deep (as in solar cells), the differences between the erfc and the Gaussian distribution are negligible.

b. *Liquid Dopants.* The diffusion of liquid dopants to form junctions is similar to gaseous diffusion. Liquid dopants are normally formed by placing the dopant and glass-forming compounds into solution with organic solvents. The commercial formulations are proprietary, but the key objective is to have the dopant in a liquid solution so that when the solution is placed on the wafer surface (by spraying, spinning, or coating) and the solvents are driven off, a dopant glass or film remains on the silicon surface (similar to the deposition step in gaseous diffusion). The dopant is then thermally driven into the silicon wafer (the same as the drive-in step in gaseous diffusion). The time-temperature drive-in parameters are similar for liquid dopant processes and gaseous diffusion processes.

c. *Ion Implantation.* Ion implantation is a third major means of forming junctions. Ion implantation differs from solid-state diffusion and is characterized by bombardment with dopant ions and subsequent penetration of the dopant into the semiconductor material. This ion bombardment usually results in crystal damage and degradation of the semiconductor characteristics. These characteristics can be recovered by high-temperature annealing. The impurity profiles obtained by solid-state diffusion and by ion implantation are also different. Solid-state diffusions (gas diffusion and liquid dopants described above) generally yield dopant concentration profiles ranging from erfc to Gaussian distribution with dopant peaks occurring at the surface. Ion implantation profiles, by contrast, generate peak concentrations at some specific penetration depth (not at the surface). The dopant distribution is essentially Gaussian at this specific peak penetration depth. However, deep dopant penetration caused by "channeling" can and does occur. In a channeling event, an atom with high energy can readily move between atoms aligned in the close-packed directions. Because the injected ion makes only a glancing collision with the channel wall, the total energy lost per unit distance traveled is small and deeper penetration occurs.

The analytical treatment of diffusion in semiconductor material is complex, but well documented in the liter-

ature. Figures 8 and 9 show typical curves of Gaussian and erfc distribution of diffused semiconductor material. Figure 10 shows a dopant distribution of ion-implanted boron and phosphorus ions. These three figures (8, 9, and 10) were taken from Reference 18, which is highly recommended for information on basic semiconductor technology as are References 19 through 22.

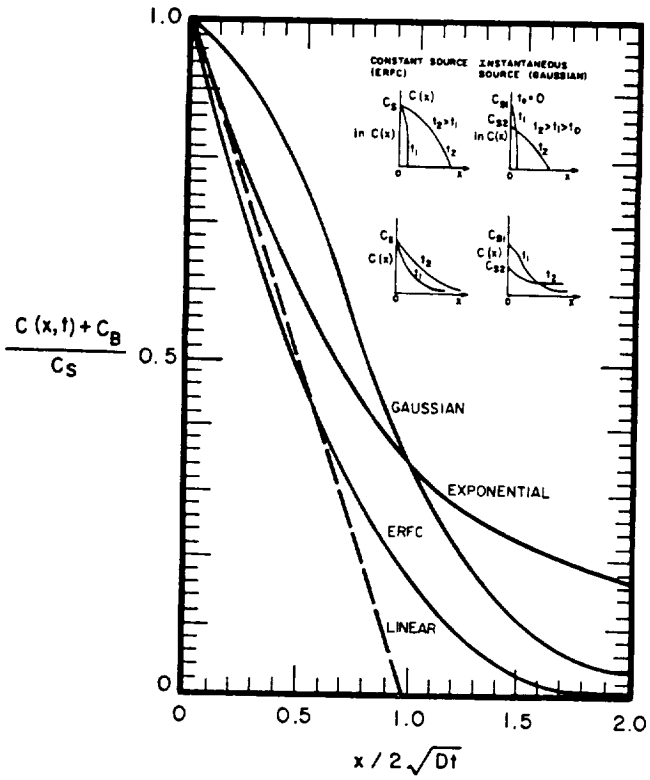


Figure 8. Ratio of Impurity Concentration at Distance x from Semiconductor Surface [C(x)] to Surface Impurity Concentration (C_O) Versus Normalized Distance from Surface. (The inset shows the variation of impurity profiles with diffusion time for the two major types of diffusion (erfc and Gaussian distribution) on logarithmic and linear scales)

The junction formation contracts awarded by the Process Development Area generated much empirical data, but it should be kept in mind that these data were based on well established theory and technology. The thrust of these contracts was not to generate any new theories, but rather to evaluate the cost effectiveness of various junction-forming technologies.

C. PROCESS DEVELOPMENT

1. Junction Formation by Spray-on of Liquid Dopants

Sensor Technology (Reference 23) demonstrated junction formation using a spray-on technique of liquid

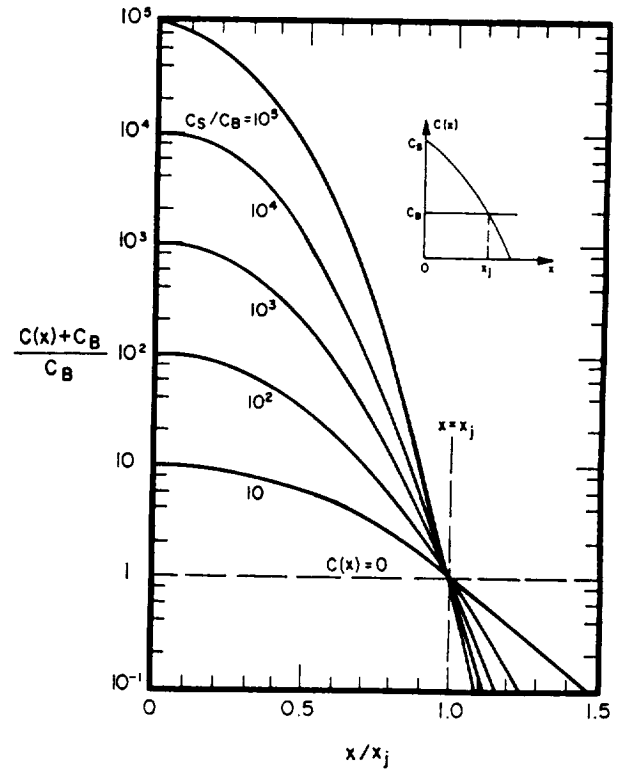


Figure 9. Impurity Concentration [C(x)] at Distance x Normalized with Respect to Background Impurity Concentration (C_B) Versus Distance from Semiconductor Surface (x) Normalized with Respect to Junction Depth (x_j) for Various Ratios of Surface Impurity Concentration (C_O) to Background Impurity Concentration

dopants. Both a front and a back junction were generated by a spray-on technique. The spray-on equipment was designed and constructed by Advanced Concepts Equipment. The system was specifically designed to spray thin-film liquid dopants onto silicon wafers. The spray-on system is shown in Figure 11.

a. *Operation of the Spray-on Equipment.* The spray-on system was capable of processing about 1 ft^2 of silicon surface per minute and allowed a 65% use of dopants. The spray chamber housed an air atomization spray gun that dispensed both the dopants and cleaning solvents. The spray gun was directed to dispense the liquids across the silicon wafers as the wafers were conveyed by a conveyor belt through the spray chamber. This resulted in overlapping passes of dopants on the wafers, thus ensuring complete coverage.

The sprayed cells were directed to an infrared (IR) oven where the cells were baked to form a dopant glass. Drive-in temperatures were done at elevated temperatures, ≈850 to 900°C. Spray-on back surface junctions (p^+) were first formed on p-type wafers and then followed by spray-on front junction (n) formation.

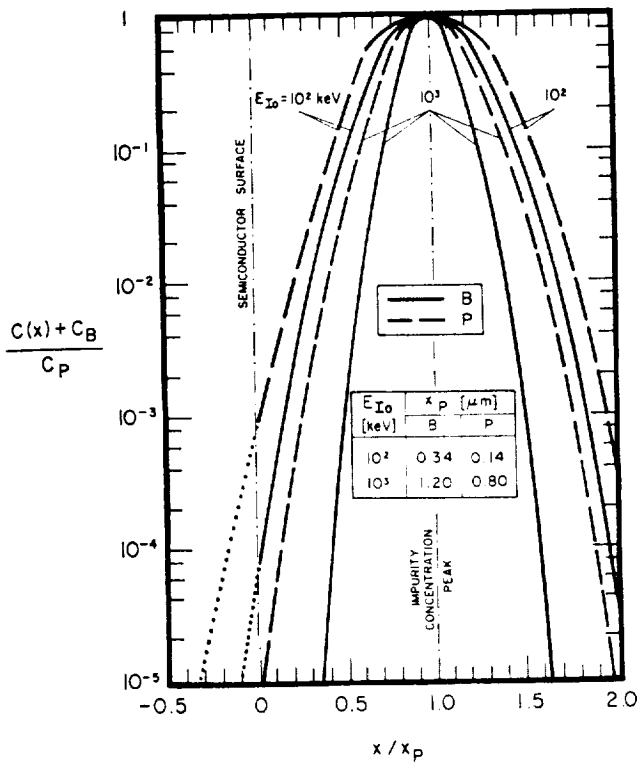


Figure 10. Impurity Concentration [C(x)] at Distance x from Semiconductor Surface Versus Distance from Surface (x) and Location of Purity Concentration Peak (x_p). (Boron and phosphorus in silicon at 300 K. This illustration shows the impurity concentration as a function of normalized distance from x_p where the semiconductor surface is at $x/x_p = 0$ and the peak impurity concentration at $x/x_p = 1$)

The operational characteristics were as follows:

(1) The optimum nozzle speed, V_n, was 50 strokes/min at a maximum conveyor speed, V_c, of 2 ft/min.

(2) The optimum atomization pressure P_a, for a dopant flow rate of 7 cc^3/min, was 18 psi. For a dopant flow rate of 10 cc^3/min, P_a was 25 psi.

(3) The optimum baking temperature, T_0, for all test conditions was 375°F.

(4) The optimum nozzle diameter, D_n, for both N and P dopants was 10 mils.

The liquid dopants used in the spray-on process by Sensor Technology were Emulsitone N250 (a water-based phosphosilica film for the front junction), and Emulsitone borosilica film (a water-based compound for the back junction). The spray-on effort is described in Reference 23.

2. Junction Formation by Spin-on of Liquid Dopants

Spectrolab (Reference 24) approached the problem of junction formation by use of liquid dopants and spin-on techniques. The spin-on technique employed commercial off-the-shelf equipment used in the semiconductor industry. Liquid dopant sources for the N layer (on P-doped silicon) were the N-250 dopant by Emulsitone Co., Whippany, New Jersey, and PX-10 dopant from Allied Chemical. Spectrolab also investigated solid diffusant sources such as the Transene 1029N Phosphorus Diffusant Preform from Transcene Co., Rowley, Massachusetts. Of the three, the best cells were made with PX-10 liquid dopant. Spectrolab also investigated spray-on techniques. Again, the best cells were made using PX-10 dopant. However, the Spectrolab technique for spraying on a liquid was with a hand-held air brush, not a full-blown prototype spray machine such as that used by Sensor Technology. Although most of the data collected on front junction formation were with spin-on dopants, Spectrolab recommended a spray-on process for front junction formation because it was determined to be more cost effective.

3. Aluminum-Printed Back Junction Formation

Spectrolab (see Reference 24) also investigated p^+ back junction formation, and recommended a printed aluminum p^+ back contact in its process sequence. Some of the procedural changes in the back junction processing included not removing the diffusion oxide prior to printing the aluminum back contact and exercising caution in eliminating sources of contamination (e.g., tooling, fixtures, etc.). Warpage of its cell because of differences in thermal expansion of silicon and aluminum was reduced by printing a grid pattern, rather than having full coverage on the back of the cell. The aluminum firing cycle was shown to be compatible with the printed front contacts. The aluminum cycle was fired separately, but did not degrade during the front contact firing cycle.

The Spectrolab investigation with aluminum pastes was extensive. A review of any silicon/aluminum phase diagram illustrates the logic of the firing cycle. The printed wafer is heated to 750 to 900°C; the aluminum melts and dissolves silicon to about 22 to 33 at. %. Upon subsequent cooling, silicon solidifies and is heavily doped (saturated) with aluminum. Continued cooling decreases the silicon content of the melt until eutectic composition and temperature is reached, where an intimate mixture of aluminum and silicon phases form. Spectrolab also determined that results were better when the aluminum paste was fired in an oxidizing atmosphere where the outermost particles oxidized and sintered together to form a crust that prevented a puddling action in the underlying molten layer.

Aluminum pastes that were used in the Spectrolab work included Alcoa 1401 paste and Englehard 3484A aluminum paste. Spectrolab also used its own aluminum paste with good results. This paste was fabricated by mixing Alcoa 1401 aluminum powder with solvents and binders purchased externally.

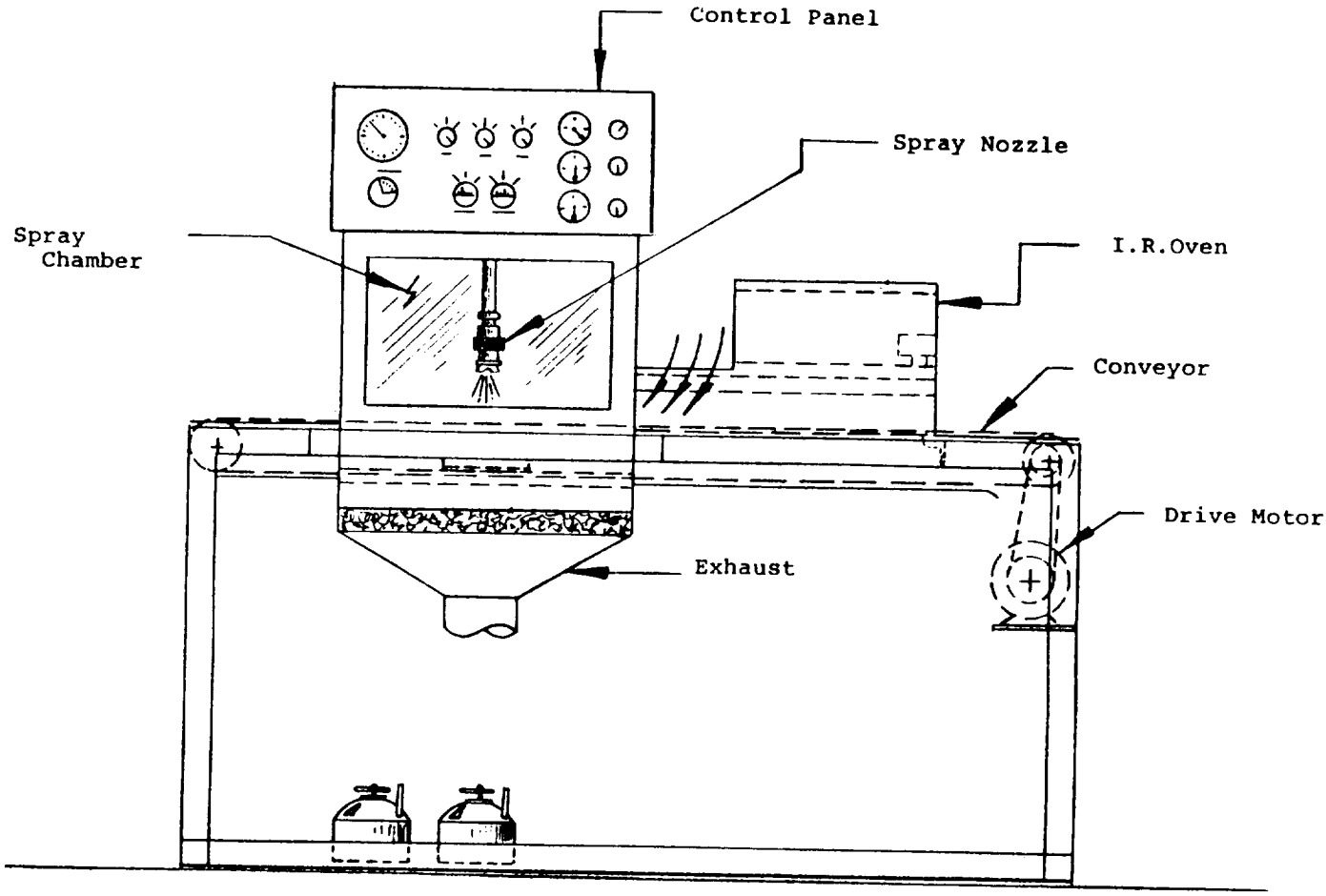


Figure 11. Spray-on Dopant System Model

The open-circuit voltages that Spectrolab obtained on their back junction work were some of the highest V_{OC} (610 mV) attained in the industry during the Process Development Area timeframe (1978 to 1980). The Spectrolab final report, which was very extensive and well written, covers all processing work including junction formation during the Process Development Phase II, and is presented as Reference 24.

4. Gaseous Diffusion Junction Formation

All Process Development Area contractors used gaseous diffused junctions for their baseline or control cells when they were developing other junction forming techniques or other process steps (metallization, assembly, etc.). The two commonly used gaseous diffusants for front junctions were $POCl_3$ and PH_3 gases. Motorola and Spectrolab used PH_3, for example, in their baseline work while Westinghouse, ASEC, and RCA used $POCl_3$ for their baseline work. Only Westinghouse proposed gaseous diffusion as a junction-forming process step in a low-cost process sequence able to meet the Project's $0.70/W module goal. Analyses indicated that gaseous diffusion processes to form junctions could be made cost effective through large-volume production equipment. The Westinghouse Process Development work is reported in a Final Report 954873 (Reference 25).

5. Liquid Dopant Coating

In addition to the liquid dopant spin-on work by Spectrolab and the spray-on work by Sensor Technology, Westinghouse, which had previously been attracted to high-volume gaseous diffusion, investigated the use of liquid dopants on dendritic web silicon. Their investigation led to the replacement of its baseline gaseous diffusion process with liquid dopants to form front and back junctions. The company also investigated techniques for applying liquid dopants. A machine using a meniscus coating technique was developed by Integrated Technologies under subcontract to Westinghouse. Figure 12 is a schematic drawing of the meniscus coating technique. Referring to Figure 12, the fluid is applied to a porous applicator, and the substrate (web) is drawn across the top of the applicator where it forms a meniscus with the fluid. The machine performed well and has applications for AR coatings, photoresist coatings, and liquid diffusion masks, in addition to liquid dopants. The report on the liquid dopant coating work, including sequential simultaneous junction formation, is reported in the referenced Westinghouse final reports (References 26 and 27).

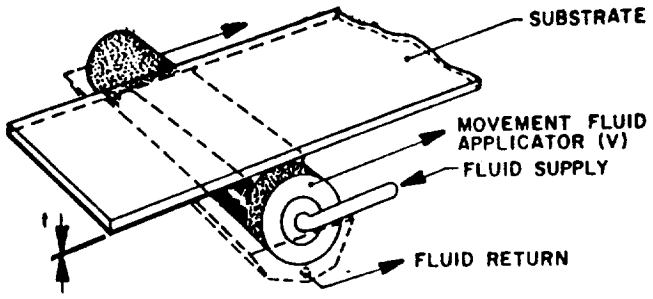


Figure 12. Meniscus Coating of Precursor Fluids to Dendritic Web Silicon

6. Ion Implantation

Most of the major ion implantation work on solar cells was done by Spire Corp. Their work (Reference 28) demonstrated a state-of-the-art solar cell implanter that processed 300 3-in.-diameter wafers per hour. Implantation parameters were 2×10^{15} $^{31}P+$ ions cm^{-2} for the front junction, and 5×10^{15} $^{11}B+$ cm^{-2} for the back junction. Silicon starting material characteristics were 10 ohm-cm (100 orientation), Cz, p-type, and 12 mils thick. The ion bombardment crystal damage was removed through thermal annealing. Cell efficiencies were 14 to 15%, at AM 1. The ion implanter, designed and built by Varian/Extrion, was modified by Spire Corp. for the specific requirements of solar cell fabrication. Spire also covered preliminary modeling studies on PEBA. They recommended that ion implantation and pulse annealing be integrated into a single-junction processor. They also recommended development of a non-mass analyzed (NMA) ion implanter.

7. Non-Mass-Analyzed Ion Implantation

Investigation of a NMA ion implantation system was conducted at JPL, California Institute of Technology (Caltech), Spire, and Motorola. The conclusions resulting from these investigations were that solar cells could be ion implanted without the need for analyzing the ion mass. Cells implanted with NMA ions performed as well as cells implanted with mass analyzed ions. The conclusions were significant to the PV industry because it simplified the ion implantation process and provided direction for future funding in ion implantation development for solar cells.

Motorola, Inc. included ion implantation for front and back junction formation in its process sequence development. An ion milling machine was used to demonstrate the efficacy of ion implantation. The ion beam was NMA. The company was able to demonstrate cells of approximately 12% efficiency on 3-in.-diameter cells. The writeup of Motorola's ion implantation work is documented in a final report (Reference 29).

8. Ion Implantation of Silicon Sheet Materials

Most of the ion implantation work accomplished in the earlier part of the FSA program used Cz single-crystal silicon because of the unavailability of sheet silicon material. A contract was awarded to Spire Corp. in 1983 to evaluate ion-implanted sheet silicon materials that had become available. The sheet materials included: (1) dendritic web, (2) edge-defined film-fed (EFG) ribbon, (3) heat exchange method (HEM), (4) semicrystalline casting process material from Semix, Inc., and (5) Silso™ material from Wacker-Chemitronic. Ion-implanted cells from each of the five sheet materials showed efficiencies comparable to or better than standard gaseous-diffused cells. Cell data and ion implantation and annealing characteristics are presented in the Spire final report (Reference 30).

9. Pulsed Electron Beam Annealing

Ion implantation requires an annealing step to activate implanted ions, i.e., to move the ions from interstitial locations in the silicon lattice to a covalent bonding position with the silicon atoms. Furnace annealing was the established means for activating implanted ions. Under Spire Contract 9547861, completed in April 1979, it was demonstrated that pulsed electron beams could be used to activate implanted ions and yield finished cells of comparable performance to furnace-annealed cells. What was not demonstrated was the throughput capability of electron beam anneal to make it a cost-effective process. A later contract, 955640, was awarded to Spire to design, build, and demonstrate an electron beam processing capable of annealing 10^7 4-in. wafers per year. Although the contract goals were reduced because of budget limitation, an electron beam pulser was successfully demonstrated to anneal 4-in.-diameter wafers at a rate corresponding to 10^7 wafers per year. An NMA ion implanter was also demonstrated to produce comparable quality solar cells. The final contract report, 955640, describes the technical details of the electron beam pulser, and presents empirical data on beam annealing and NMA ion implants. The final report is identified as Reference 31.

10. Excimer Laser Annealing

Under a special DOE funding agreement, JPL was directed to investigate the efficacy of excimer lasers to anneal ion-implanted cells. Two contracts were competitively awarded, one to Spire Corp. and one to ARCO Solar Corp. Both contractors produced cells of comparable (but slightly lower) quality relative to furnace-annealed cells. The Spire conclusion was that excimer laser anneal is not cost effective in annealing solar cells relative to furnace annealing. ARCO Solar also produced annealing data that indicated marginal cost effectiveness of excimer laser annealing. At ARCO Solar, excimer laser investigations of deposition of metals and passivation films were not successful.

Excimer lasers were also investigated by Westinghouse to drive-in liquid dopants to form front and back junctions. Front junction formation by excimer lasers using phosphosilicate films was good, producing junction profiles comparable to furnace drive-in. Profiles of the back junction were not good, lacking adequate depth. However, the consensus was that excimer lasers with adequate research could be applied for

liquid dopant drive-in to produce both front and back junctions successfully.

The excimer laser studies are described in the following final reports: Spire (Reference 32), ARCO Solar (Reference 33), and Westinghouse (see Reference 27).

11. Nd:Glass Laser Annealing

Lockheed Corp. investigated annealing in implanted cells using a Quantel 30-J, 20- to 50-μs, Q-switched Nd:glass laser equipped with a frequency doubler that permitted operation at 1.06- and 0.53-μm wavelengths. Results showed that cells could be annealed with AM1 conversion efficiencies up to 15.4% for 4-cm^{-2} cells and up to 14.5% for 7.6-cm-diameter cells. The company reported its best results with ion implantation conditions of $^{31}P^{+}$ implants at 5 keV and a dosage of 2.5 $\times$ 10^{15} ions/cm^2, using a laser energy density of 1.5 J/cm^2 and a 20-μs pulse duration.

Experiments also showed that texture-etched surfaces are not compatible with pulsed laser annealing because of surface melting caused by the laser energy. Lockheed also generated empirical data showing the differences in the dopant concentration profile as a function of depth when the laser anneal energy density was changed. The dopant profiles are shown in Figure 13. The Lockheed laser anneal work is described in Reference 34.

12. Module Experimental Process System Development Unit Junction Formation

Two MEPSDU contracts were competitively awarded to Solarex and Westinghouse in late 1980 to provide the first controlled pilot line data on cell processing for low-cost module fabrication. Because these two contracts reflected the technology gained from the earlier process development contracts, the selection of the junction forming techniques is noteworthy. Solarex selected spray-on dopants for front junction formation and a screen-printed aluminum paste for the back junction. Westinghouse selected gaseous diffusion for its front junction and boron diffusion for its back junction. Solarex settled on ion milling to isolate the front and back junctions. Westinghouse selected laser scribing for junction isolation. The MEPSDU junction formation efforts are described in the Solarex final report (Reference 35) and in the Westinghouse final report (Reference 26).

13. Rapid Thermal Processing

RTP, obtained by the use of heat lamps, is a rapidly growing method of annealing ion-implanted wafers in the semiconductor industry. The process works by exposing wafers to a tungsten filament or argon arc lamp for seconds or minutes, at most, thereby raising the wafer temperature sufficient to activate the dopant ions and anneal the damage. The RTP annealing process requires only a fraction of the time that furnace annealing does. Westinghouse investigated the RTP process for driving in liquid dopants to form front and back junctions simultaneously. The results of this investigation

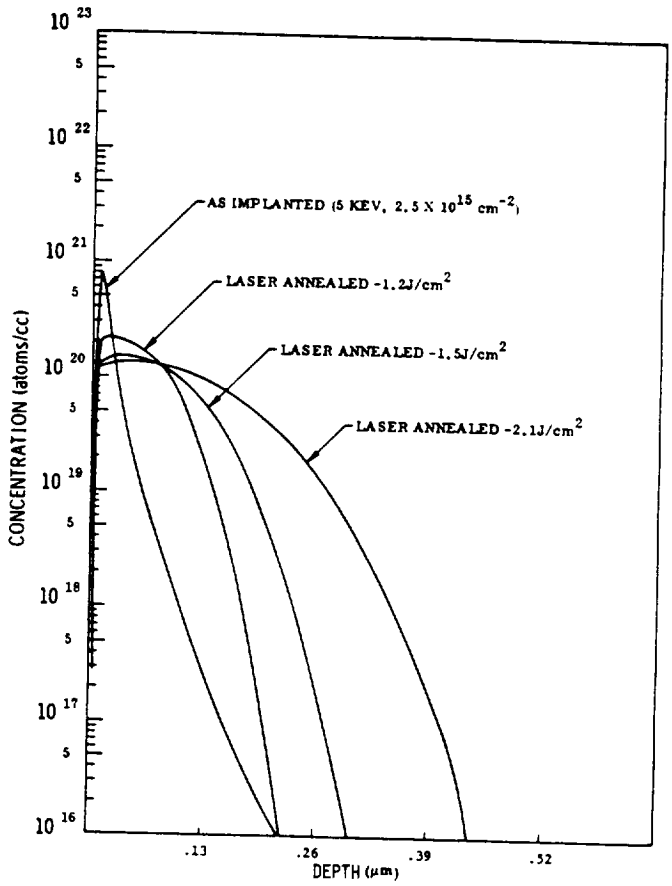


Figure 13. SIMS Profiles of 5-keV Phosphorus in Silicon for as-implanted and Laser Annealed Specimens

were good. It was demonstrated that simultaneous front and back junctions could be formed that would produce cells equal to or better than the performance of cells produced by the baseline process which formed junctions sequentially by furnance drive-in. The Westinghouse best cells, in excess of 15% efficiency, were made with n-type silicon dendritic web material. The results of this work with RTP are published in the Westinghouse final report (see Reference 27).

D. RELIABILITY

Once the junction is formed and properly isolated, its reliability, in terms of functioning, is high and essentially does not change under normal environmental conditions experienced by solar cells. The issues of process control in a mass production environment and the reliability of junction characteristics as a function of time were not fully addressed during the life of the FSA Project.

E. ECONOMICS

The economics of junction formation was determined by a standard cost methodology developed early in the FSA program. All Process Development Area contractors were obligated by contractural requirements

to fill out Format A's for each process step. The Format A's were costing sheets for inputting cost details such as equipment, direct labor, material, floor space, and utilities. The Format A data were then inputted to a main frame computer to run the JPL SAMIS computer program for consistent process costs.

In addition to SAMIS, a smaller, simpler costing standard was used, called Interim Price Estimation Guideline (IPEG). This costing system was simple enough to be executed on a hand calculator. It used standardized coefficients for costing inputs such as equipment, direct labor, material, floor space, and utilities. The IPEG method was used on an interim basis to provide ball-park costing information during the contract period.

A third document, called SAMICS, which is a catalog of material costs, labor costs, and other costs, was used to provide data for inputting standardized costs into the IPEG and SAMIS programs.

Some of the junction formation costs gleaned from the FSA final reports include:

(1) Sensor Technology: Spray-on liquid dopants, $0.031/W (1975 dollars). The costs covered front and back junction formation for dopant spray-on, dopant drive-in, and excess dopant removal (see Reference 23).

(2) Westinghouse: $POCl_3$ gaseous diffusion, front junction, $0.056/W (1980 dollars); boron (B) back surface field (BSF), $0.058/W (1980 dollars) (see Reference 25).

(3) Solarex Corp.: Spray-on front junction, $0.0565/W; Al paste, BSF, $0.0344/W; back junction cleanup, $0.0593/W (1980 dollars) (Reference 35).

(4) Spectrolab: Spray-on front junction, $0.0136/W; Al BSF, $0.0097/W; cleanup $0.0078/W (1980 dollars) (see Reference 24).

(5) Spire Corp.: Ion implantation, total front and back junctions including annealing, $0.041/W. Figure 14 shows the junction costs versus production quantity. (See Reference 31 for writeup of costs.)

(6) Motorola Inc.: Advanced ion implantation, $0.014/W (see Reference 29). (Note that Motorola's costs were taken from the Technology Assessment Report before SAMICS was used.)

(7) RCA: Ion implantation, $0.026/W (Reference 36).

F. KEY ACCOMPLISHMENTS

The following list summarizes some of the key accomplishments in junction formation that were achieved during the FSA Project's lifetime:

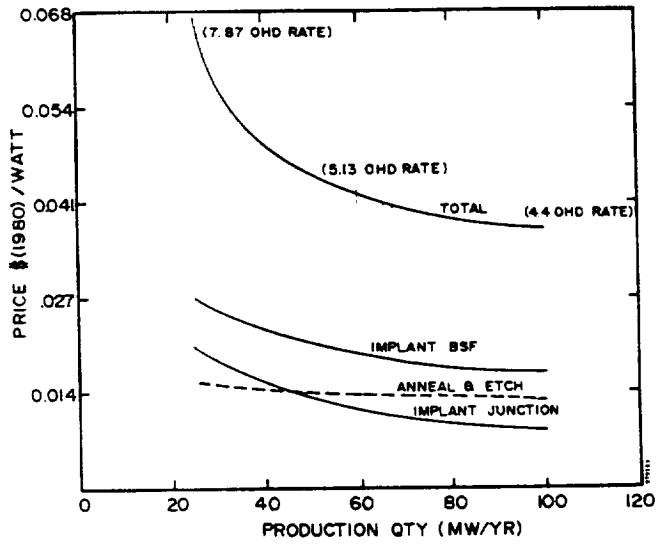


Figure 14. SAMIS III Cost Estimates for Junction and Back Surface Field Formation (Spire Corp.)

(1) Large-area, large-volume, gaseous diffusion processing using $POCl_3$, PH_3, and BBr_3 (Sensor Technology and Westinghouse).

(2) Simultaneous front and back junction formation using liquid dopants RTP techniques (Westinghouse).

(3) Ion implantation of both front and back junctions at a rate of 300 wafers/hour (Spire).

(4) NMA ion implantation of both back and front junctions (JPL, Motorola, and Spire).

(5) Laser annealing, PEBA, and rapid thermal pulse annealing of ion-implanted junctions as well as conventional thermal annealing to maintain lifetime of the initial silicon material (Spire, ARCO Solar, and Lockheed).

(6) Spin-on, spray-on, and meniscus coating of liquid dopants (Spectrolab, Sensor Technology, and Westinghouse).

(7) Laser scribe (Sensor Technology and Westinghouse).

G. CURRENT STATUS

The present status of junction formation is that gaseous diffusion continues to be the workhorse technique for forming junctions for routine and small production lots. Meniscus liquid dopant application, followed by heat lamp drive-in, seems to have the best potential for near-term implementation. Non-mass ion implantation followed by furnace anneal is also being used for small production lots of solar cells.

H. REQUIRED FUTURE TECHNOLOGY NEEDS

The one single technology need for junction formation is the development and verification of large-volume junction formation equipment. All of the cost analyses indicate a cost-competitive posture for solar cell manufacture and specifically for junction formation. However, these cost analyses were and are based on extrapolated data. A conversion to mass production is needed (as planned in Phase V of the Process Development Area) to obtain cost data generated by large-volume production equipment and to verify extrapolated costs.

SECTION IV

Metallization

A. BACKGROUND

In the fabrication and interconnection of semiconductor devices, metal systems are relied upon to perform a variety of distinct functions. In addition to forming the link between the semiconductor material and the external circuit, metals may be used to aid in the dissipation of heat, to shield the device from the existent environment, or to form an inherent part of the device through the electrical properties of the interfaces. The composite-defined film described above is the semiconductor metallization system.

The problems encountered in attempting to find a suitable metallization system for a semiconductor application are varied. The specific conditions of an operating system are diverse. In this specific system, the problems are operating temperature, reliablility, and economics.

In choosing an appropriate metallization system for a specific semiconductor application, the first question to be addressed is that of functional requirements. These can be divided into three rather rough categories: (1) device processing considerations, (2) device reliability considerations, and (3) economics. The most important and most universal of these considerations are:

(1) Processing

  (a) Compatibility with practical metal deposition methods (evaporation, sputtering, plating, and screening).

  (b) Adhesion of the sandwich system (i.e., metal to silicon).

  (c) Compatibility to the required metallization patterning system.

  (d) Compatibility to the thermal cycling during processing (critical in this application).

  (e) Compatibility with subsequent cell-to-cell interconnecting techniques.

(2) Reliability

  (a) Resistance to interdiffusion of metal with substrates and interconnecting layers during processing.

  (b) Resistance to the formation of degrading intermetallic compounds during subsequent use.

  (c) Resistance to electromigration, again, during use.

(3) Economic

The material and processes used to form these systems must be compatible with the overall FSA cost goals.

The effects of high-temperature processing on cell performance need more study, unless a large amount of statistical data are generated which usually is not economically feasible. This dictates that the metallization system chosen for the unique requirements of terrestrial PV cells be well understood.

An initial Assessment Phase was competitively awarded to three contractors: RCA Laboratories, Texas Instruments, and Motorola, Inc.

The goal of the study was an assessment of existing processing technologies as applied to the manufacture of solar modules. It also involved comprehensive assessments of the existing technology that might be needed to develop, within a period of no more than 10 years, an industrial capability for low-cost, mass production of durable silicon PV modules and arrays. This assessment defined the current state-of-the-art processes available to produce cells and modules from given silicon inputs. It stimulated the adoption of a standard methodology that allowed: (1) relative comparisons of the potential price attributable to competing processes, and (2) a best possible estimate of the actual price obtainable from a process. The SAMICS represents such a methodology which was subsequently developed and has been continually updated. It supplies credible standards for financial assumptions, including prices of material and labor, a methodology for overhead estimation, and an unambiguous format for the description of a process.

In the context of the solar cell process costing assessment, all three contractors concluded that the cell metallization process was the single most expensive step in the manufacturing sequence. Specifically, the material cost of the conductive metal seemed to be the limiting factor in reducing metallization costs.

The three contractors developed similar approaches to solar cell metal pattern design, using mathematical models with minimum power loss as the governing parameter. These models for optimized metallization patterns were used in the evaluation of front-side metallization technologies. Their outputs were a significant factor in pursuing developmental processes for baseline low-cost process sequences.

B. THEORY

1. Metal Semiconductor Interfaces

The role of the metal semiconductor interface has been under active investigation since 1874 when K.F. Braun (Reference 37) first discovered that such an interface carried current more easily in one direction

than another. The structure of this basic interface was first described by Schottky (Reference 38) and Mott (Reference 39). A simple explanation will be given using Figure 15 from Rhoderick (Reference 40).

In an ideal metal semiconductor system, the potential barrier height is primarily determined by the work function difference between the metal and the semiconductor. The shape of this barrier is determined by a uniform space charge caused by ionized impurities.

This can best be explained by examining Figure 15. Suppose that, as shown in Figure 15(a), the metal and the semiconductor are both electrically neutral and separated from each other. In Figure 15, ϕ_m is the work function of the metal; ϕ_S is that of the semiconductor. Some definitions are given in the following paragraphs.

a. *Work Function of a Metal.* As shown in Figure 15(a), the thermionic work function of the metal is ϕ_m, which is defined as the energy required to remove a conduction electron from the Fermi level of the metal to the vacuum energy level.

$$\phi_m = (E_o - E_F^m)\,(q)^{-1}$$

b. *Work Function of a Semiconductor.* Similarly, the thermionic work function of a semiconductor, ϕ_S, is defined as the energy required to remove an electron from the Fermi level of the semiconductor to the vacuum energy level.

$$\phi_x = X_S + E_G\,(2q + \phi_F)^{-1}$$

where X_S is the electron affinity of the semiconductor, the energy required to remove an electron from the bottom of the conduction band to the vacuum energy level, and ϕ_F is the Fermi potential, which is measured from the Fermi level to the conduction band and is in itself a function of impurity concentration.

c. *Barrier Height.* The barrier height of the metal semiconductor system, ϕ_{ms}, can be predicted by two models, depending upon the magnitude of the surface-state density. One is the work function model, known as the Schottky-Mott model. The other is the surface-state, or more recently referred to as the "defect" model.

Schottky-Mott Model. The work function model assumes that the surface-state density is negligible and the barrier height is determined by the difference in the work functions of the metal (ϕ_m) and semiconductor (ϕ_S). This brings us back to Figure 15.

As shown in Figure 15(a), the metal and semiconductor are both electrically neutral and separated by a gap. The energy-band diagram depicts an n-type semiconductor with a work function less than that of the metal ($\phi_m > \phi_S$). If the metal and semiconductor were connected with a wire externally, electrons would flow from the semiconductor to the metal and the two Fermi levels would be forced to be equal (coincident). The energies of the electrons at rest outside the surfaces of the two solids would be no longer the same, and there would be an electric field in the gap directed from the right to the left. There must be a negative charge on the surface of the

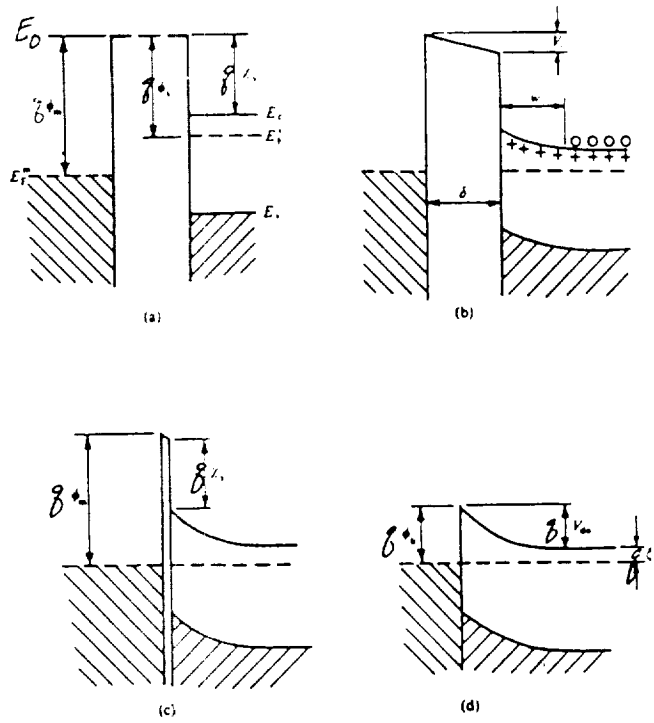


Figure 15. Formation of a Barrier Between a Metal and a Semiconductor

metal, balanced by a positive charge in the semiconductor. In an n-type semiconductor, the positive charge is provided by ionized positive-charged donors in the region depleted of electrons (the depletion region). Because the donor concentration is many orders of magnitude lower than the electron concentration in the metal, this depletion region extends to an appreciable thickness (w) and the bands in the semiconductor are bent upwards as shown in Figure 15(b). In the case of intimate contact as show in Figure 15(d) where there is no gap separating the metal and semiconductor, the barrier caused by the vacuum gap disappears and the barrier height, ϕ_b, measured relative to the Fermi level, is given by

$$\phi_b = \phi_m - X_S$$

Surface-State Model. The surface-state model assumes that the surface-state density of the semiconductor surface is large ($Q_{ss}/q > 10^{14}\text{cm}^{-2}$) and the Fermi level pins at the predominant surface-state level. In this case, the barrier height is determined by the location of the surface-state level and is independent of the properties of the metal and the impurity concentration of the semiconductor. It has been empirically found that for an n-type semicondutor, $\phi_b \equiv (1/3)E_G$, which holds qualitatively for several different metal contacts on some common semiconductors.

In actual practice, the system appears as shown in Figure 15(c) where the indicated small gap is a thin insulating layer of oxide, some 20 Å thick on the surface of the semiconductor. The effect of these surface states has been shown (Reference 41) to influence the measured barrier height by screening the interior of the semiconductor from the metal. This accounts for the

difference in theoretically-versus-experimentally measured data. Work is continuing in search of an explanation for the effect of these surface states on device characteristics (e.g., all of the metal oxide semiconductor-based industry). Figure 16 is a plot of experimental values of heights for metals and metal silicides on n- and p-type silicon.

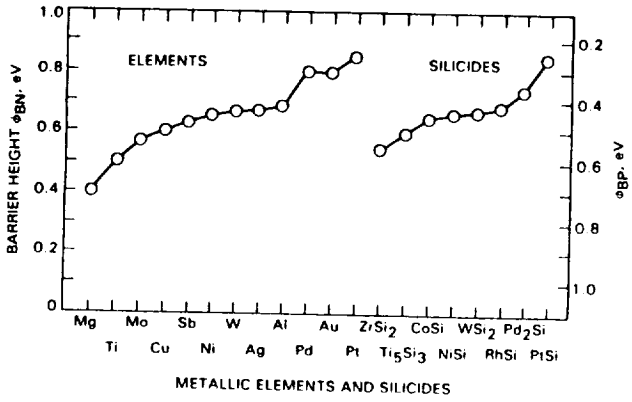


Figure 16. Barrier Heights for Metals and for Metal Silicides on p- and n-Type Silicon

The interface is critical in metal conductor systems because the charge transport mechanism involves tunneling through thin barriers between conductive carriers.

2. Real World Contacts

Experience has shown that access to a semiconductor region via a metal contact (to get the current out) usually involves a higher resistance than the ideal contact discussed above. This additional resistance may be imagined as a series resistor in the lead of the ideal cell, shown in Figure 17. Reference 42 discusses how interface layers between the metal and the semiconductor can cause non-ideal contacts.

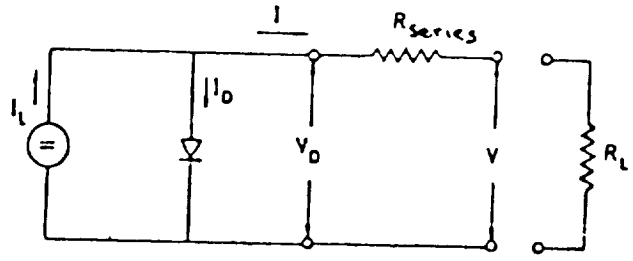


Figure 17. Simple Equivalent Circuit of a Solar Cell

This parasitic series resistance can be broken up into two components for analysis: one is contact resistance, and the other is resistance created by the dimensions and conductivity of the metal itself in relation to the physical size of the solar cell and its generated current.

From a physical viewpoint, the first parasitic loss is that caused by the contact itself. This loss can be directly attributable to the quality of the contact. The metallurgical systems and the processes used to produce low-resistance contacts to shallow junctions in silicon solar cells are the subject of the following discussion on contact resistance.

Because of the many different methods used over the years for measuring and analyzing the contact resistance, some confusion existed as to the exact definition of contact resistance. It has now been defined as the sum of the composite contributions originating at the interface and in the material underneath it. This is shown schematically in Figure 18, where R_S is the sheet resistance of the diffused layer and R_C is the contact resistance. Although the resistivity of the metal is usually very low ($>10^{-3}\ \Omega cm^2$), the current transfer from the semiconductor to the metal will take place over the transfer length, L_T.

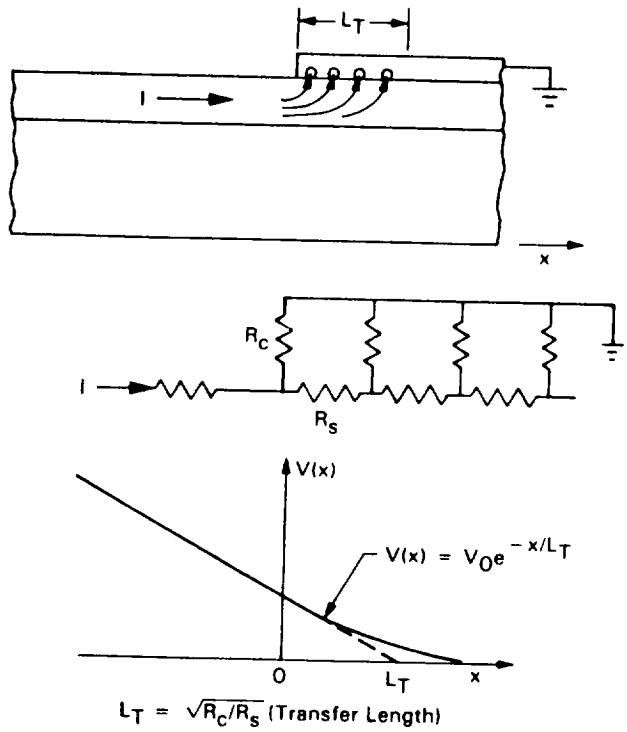


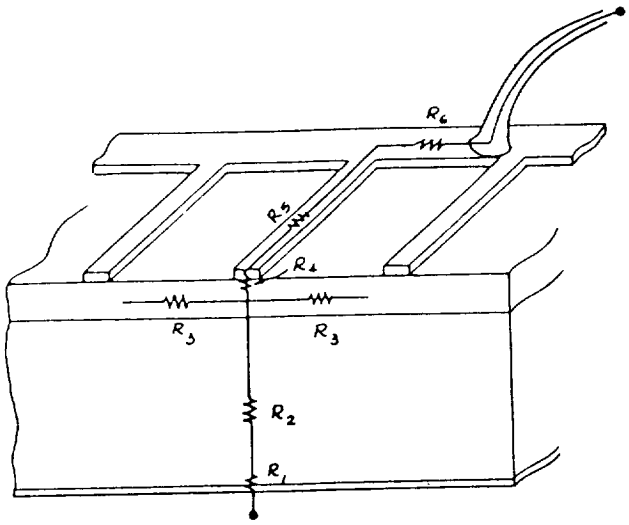
Figure 18. Contact Current Crowding

The first model and testing technique used to quantify this loss was in a transmission line technique developed by Shockley in 1964 (Reference 43). This has been elaborated by many other researchers (References 44 through 52), the most notable being that by H. Berger (Reference 44). Many test structures are available as described in these stated references, including one from the National Bureau of Standards (see Reference 48). Their mathematical derivations, including those concerned with current crowding effects, are addressed. The specific contact resistivity values evaluated are, as expected, process sensitive and vary from 10^{-3} to $10^{-7}\ \Omega cm^2$.

A solar cell requires contacts to both the n and p regions of the device for current collection. One is normally on the front surface of the device. Metal place-

ment on this surface must be in some form of a grid structure to allow sunlight to impinge on the bulk. The design of this structure involves a trade-off between power loss in the shaded active area with the metal (cell shadowing) and the dissipation in the resistive area without the metal (cell sheet resistance).

This subject has been extensively analyzed and modeled as referenced above. Figure 19 is a schematic of the resistive components addressed in these calculations. In all models, the basic approach is the same:



$$R_s = \sum_{i=1}^{6} R_i$$

R_1 = back contact R_4 = front contact
R_2 = bulk R_5 = grid lines
R_3 = diffused layer R_6 = bus lines

Figure 19. Solar-Cell Series Resistance

(1) Select J_{SC}, V_{OC}, and cell dimensions (from experience).

(2) Set up the resistor network.

(3) Compute the power-loss components.

(4) Minimize the sum of resistive and shading losses by manipulation.

(5) Estimate the operating J_{SC} and V_{OC} at various intensities under investigation.

(6) Select the optimum grid pattern (this is process sensitive).

Numerous computer programs are available and have been exercised to the point that the resistive loss models currently used are valid and can apply to large-area 1-sun operation.

C. PROCESS DEVELOPMENT

The metallization systems available in 1975 had evolved from the space cell industry. This evolution was from electroless Ni to an evaporated Ti/Ag contact to a passivated cell having a thin layer of Pd under the Ag to electrochemically passivate the Ti/Ag couple. This Ti/Pd/Ag contact system has become the standard qualified space cell metallization system against which alternatives are compared. The driving function in the FSA Project was economics. A survey of the metallization methods available was started by reviewing the Assessment Phase contracts of Texas Instruments, RCA, and Motorola (References 53 through 55, respectively). Metallization is grouped into four processing technology areas: evaporation, printing, plating, and novel approaches.

1. Evaporation

Evaporation deposition systems have been discounted on a cost basis many times, but keep reappearing because of their advantages in device efficiency and reliability already proven in space-qualified cells. Although assessed many times and used as the alternate against which performance is compared, only Westinghouse (Reference 56) uses an evaporative technique of depositing thin layers of Ti and Pd in a novel metallization system combined with an additive Cu plating operation used to provide the required conductivity. This system has been tested at elevated temperatures for its reliability, and currently is being used in the Westinghouse production facility.

2. Printing

Thick films showed the highest probability of meeting the Project's economic requirements during the Assessment Phase. The only contractor of the three involved in the Assessment Phase that chose to examine and develop thick-film technology in detail was RCA (Reference 57). They began with an analysis of commercially available Ag-based inks. Their purpose was to get the "black magic" out of this technology and make the material formulations and firing processes a science. They used emission spectrographic analysis of the material components as the basis for input material control. Using these analyses, a screen-printable Pb borosilicate-doped Ag-based ink was synthesized at RCA specifically for solar cell systems. Material constituents, electrical conductivity, solderability, and adhesion were measured as a function of ink composition and firing conditions.

Spectrolab (Reference 58) had independently concluded that thick-film screen printing of Ag for the front contact was the most cost-effective volume production technique. They had also concluded the availability of commercial production-type screen printers that could handle 6-in. substrates, were totally automatic, and had a throughput of up to 3000 substrates per hour.

Spectrolab was the first contractor to determine that the major problem with fritted glass/metal systems was the oxidative attack of the silicon. This oxidative attack of the frit/silicon interface has a time dependency that modifies cell characteristics. For very short firing cycles, high contact resistance results lead to high cell-series resistance. With increased firing time, this resistance will begin to decrease. The shunt resistance of the cell characteristic will dominate at extremes in time because of the temperature, time, and junction depth interactions. These analyses led to the optimization of the frit content and firing process and produced excellent cells (Figures 20 and 21). This process was cost effective, verified by volume throughput, and both process and economics were well documented.

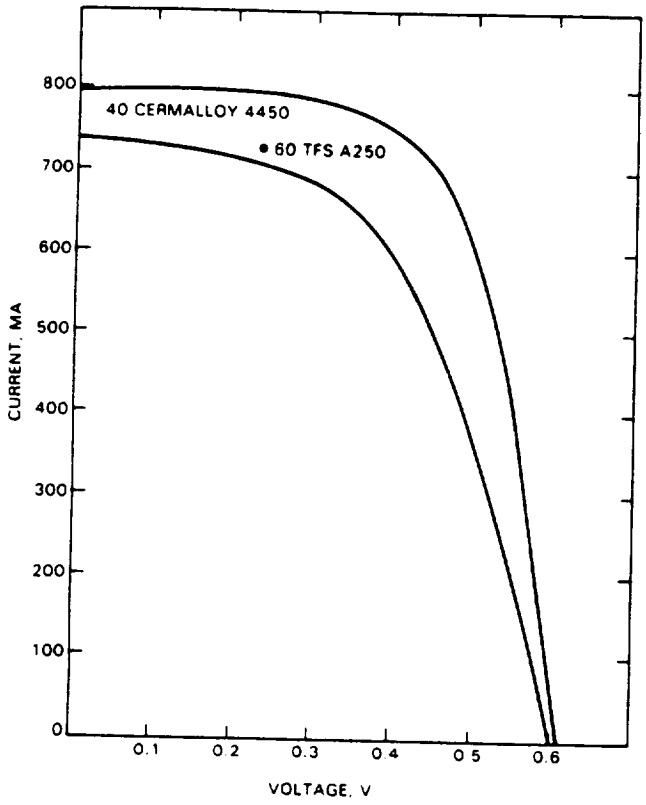


Figure 20. Improvement of Curve Shape by Reducing Frit Content of Paste

The problems involved in the use of frit (low-melting glass compositions) as the liquid-phase sintering medium led B. Ross Associates (References 59 and 60) to propose the use of a metal as the liquid-phase sintering medium. This allowed the total system to be specifically developed in regard to the choice of metal powder, vehicle, binder, and even firing atmosphere required to provide the desired mechanical and electrical properties. This, in turn, led to the development of thermo-analytical techniques to describe these complex systems as reported within the contracts themselves and by Parker and Gallagher (Reference 61).

A major contribution in the formulation of developmental ink systems to this study was made by

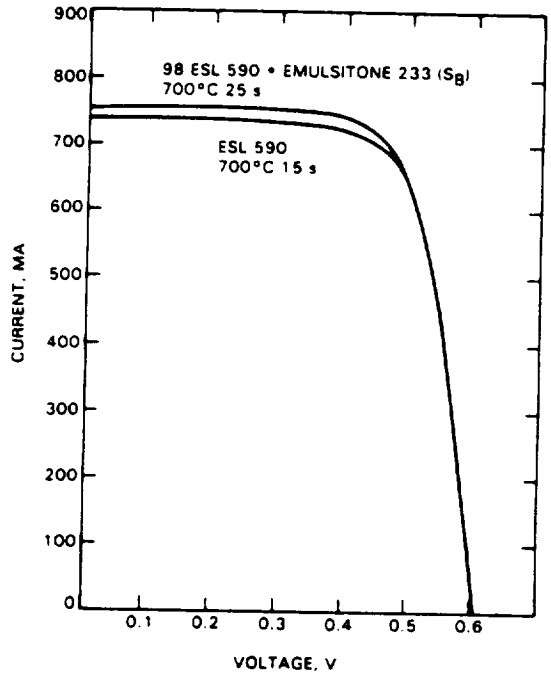


Figure 21. Effect of n-Type Diffusion Source Addition to Commercial Silver Paste on Solar Cell Performance

Electrink, Inc. These inks were designed for specific printing and firing process characteristics. As far as possible, the proprietary nature of these formulations (hitherto an industrial secret) was eliminated.

The conclusions of this contract were:

(1) Copper pastes using an all-metal concept were shown to produce good back contacts without any tendency to short the junction. Long-term reliability was not proven, and intermittent adhesion problems were not solved.

(2) When used on the front junction, this system was singularly unsuccessful.

(3) The effect of hydrogen on adhesion brought up the question of the basic nature of the bonding mechanism. An analytical technique capable of discerning empirical relationships between hydrogen concentration (number of counts), processing environment, and adhesion of the sintered metal was developed in cooperation with W.A. Langford of SUNY in Albany, New York.

SOL/LOS (Reference 62) developed a base metal system for p/n solar cells. Their approach was to select the base metal on the basis of electrical conductivity, known environmental stability, and cost.

Table 1 shows the pertinent properties of some candidate metal systems with Mo the most desirable with respect to the stated requirements. Mo has the closest match of thermal coefficient of expansion with silicon and is among the top ten in conductivity, being

Table 1. Properties of Metals

Metal	Electrical Resistivity, $\mu\Omega$-cm	Coefficient of Thermal Expansion, cm/cm/°C, 10^{-6}	Melting Point °C	Boiling Point, °C	Density, g/cm^3
Titanium	176.0	7.1	1725±10	—	4.5
Nickel	65.3	9.2	1455	3075	8.9
Lead	20.6	16.3	327	1740	11.3
Platinum	14.9	4.9	1774	4530	21.5
Tantalum	12.4	4.0	2996	4100	16.6
Tin	11.5	13.0	232	2260	7.3
Palladium	10.8	6.5	1555	3980	12.0
Aluminum	6.3	13.7	660	1800	2.82
Zinc	6.1	19.3	419	904	7.17
Tungsten	5.48	2.2	3410	5900	19.4
Molybdenum	5.17	3.1	2622	4570	10.2
Beryllium	5.0	6.4	1292±8	2980	1.84
Rhodium	4.51	4.6	1966	—	12.4
Gold	2.35	7.9	1065	2700	19.3
Copper	2.03	9.8	1083	2595	8.95
Silver	1.6	10.9	960	2000	10.5
Silicon	—	4.2	1420	—	2.33

second only to Cu among the common metals. For this reason, it is used in silicon device technology as a mechanical support as well as a heat sink. As a contacting element, it has rarely been used. Its high melting and boiling points make the film deposition by evaporation and sputtering difficult, and the pyrolytic decomposition of carbonyls or halides requires complex equipment and processing steps.

This study was based on the conversion of molybdenum trioxide (MoO_3) into metallic Mo in a reducing atmosphere at elevated temperatures. The MoO_3 is the most stable oxidation state, has a low melting point of 795 °C, and is easily reduced. In air, it sublimes at 550 °C and melts to an oily liquid at 795 °C, at which time the sublimation is extremely heavy. However, in a reducing atmosphere, the oxide reduces at 600 °C into lower oxides, mostly MoO_2, which do not sublime and can be further reduced to a dense Mo metal film. The MoO_3 is commonly available in fine powder form and, thus, is very suitable for use in a suspension adjusted for thick-film printing.

The second element chosen to form the metallization system was Sn. It was chosen for its conductivity and its good solderability characteristics as well as its low melting point.

During this contracted effort, it was proven experimentally that an ohmic contact can be obtained with silicon from a Mo/Sn metal system by reduction of a MoO_3/Sn mixture. To lower the contact resistance while maintaining the peak firing temperature at approximately 800 °C, the basic MoO_3/Sn formulation was modified by the addition of Ti in the form of titanium resinate. The effect of this addition is shown dramatically in the current-voltage (I-V) cell characteristics in Figure 22.

Spectrolab (Reference 63) transferred the above approach to n/p cells and assessed, studied, developed, and improved, in combination with a thick-film ink vendor, a Mo-based metal system. The basic ingredients of the thick-film system are Mo, Sn, and Ti hydride (TiH_2) in combination with Thick-Film Systems Vehicle 3347. The five basic combinations are given in weight percent in Table 2 and the mask layout in Figure 23.

The presence of the oxygen-sensitive Sn in the formulations required a two-step firing cycle in which the last firing required a reducing atmosphere in a tube furnace.

Rather early in the program, results were obtained that were electrically equivalent to the Ag controls. Cell characteristics are shown in Table 2 with the I-V curves

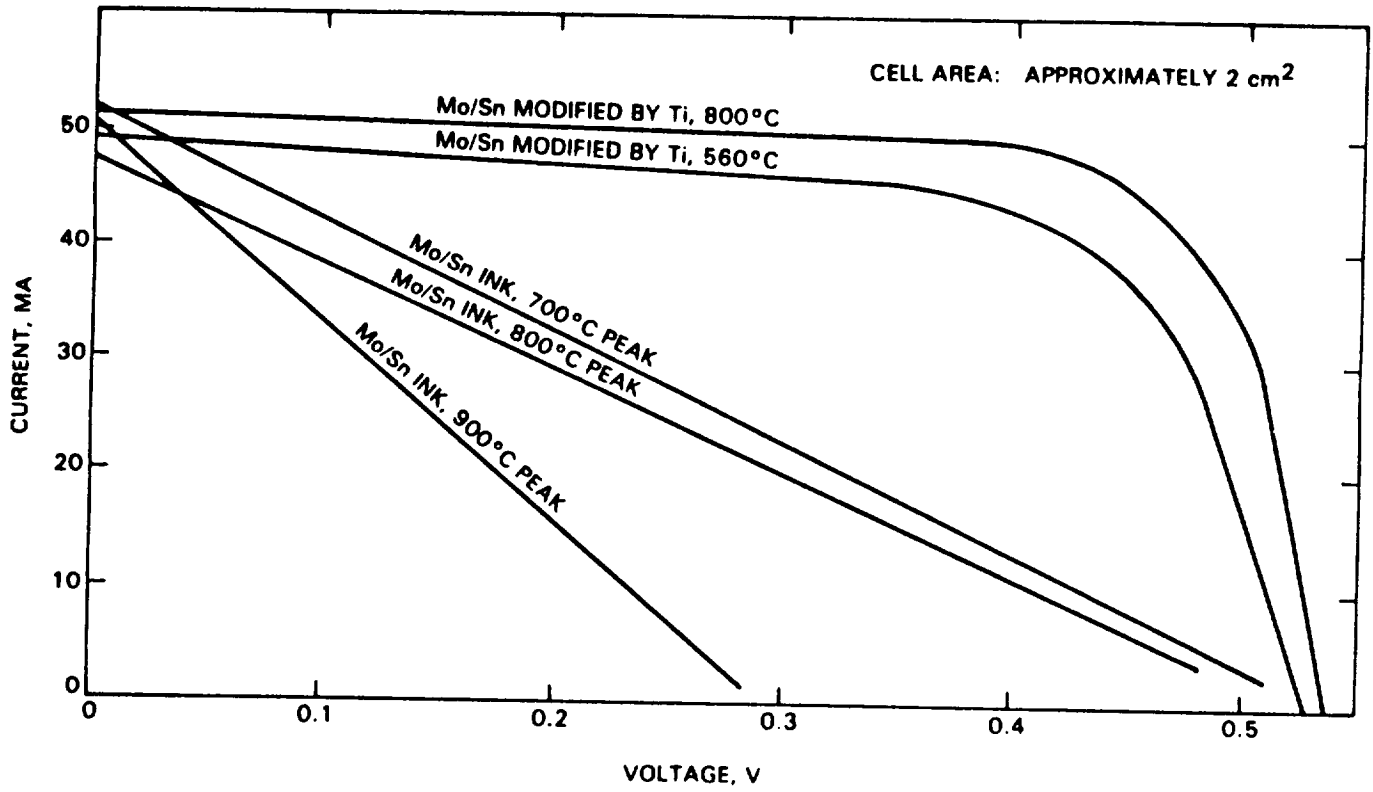


Figure 22. Current-Voltage Characteristics of p/n Cells

Table 2. Ink Compositions

Type	Sylvania 280-325 Mo	Atlantic Equipment Engineers SN 266 Sn	Ferro Plant PX-41 TiH_2
A	19.5	80.0	0.5
B	50.0	49.5	0.5
C	70.0	29.5	0.5
D	49.0	49.0	2.0
E	48.0	48.0	4.0

Note: These powders will be mixed using the vehicle from Thick-Film Systems' silver paste 3347.

at varying light intensities shown in Figure 24. Note that neither cell is AR coated.

Based on this early electrical success, a Technical Direction Memorandum (TDM) was incorporated modifying the study to include the use of indium tin oxide (ITO) as a combination antireflective coating and an additional (parallel) conducting system. The rationale was based on the fact that equivalent efficiencies were obtained with the Mo/Sn/TiH_2 formulation, even though (as shown in Figure 24) the cell has a higher series resistance. This allowed more freedom in the thickness/absorption/current-carrying characteristics required of the ITO film.

The ITO films were prepared by Applied Film Labs. Preliminary screening experiments fired the films in both hydrogen and carbon monoxide. The ITO was easily reduced in hydrogen, turned milky, and became opaque. The effect is less pronounced in carbon monoxide. The result was that these cells with ITO as an AR coating were not equivalent to the Ag metal-SiO AR coating (they are equivalent without the AR coating). This fact, coupled with the inability of the subcontractor to reproduce acceptably characterized films, caused cessation of the study.

Solderability of these systems involved a problem in reproducibility. The solderability problem was circum-

vented by using a two-step printing and firing process in which printing and firing a Ag pad was the second step. This was a technical rather than an economic solution. Again, the process specification and the economic analysis of the developed process is well documented in the referenced document.

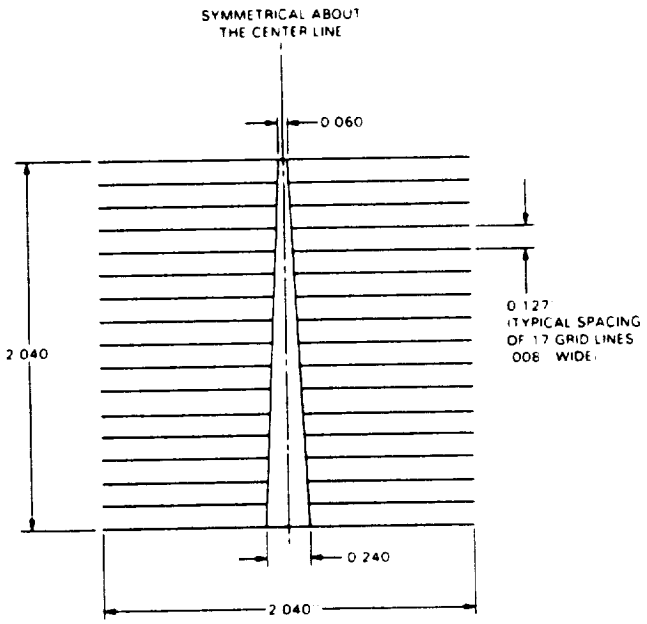


Figure 23. Front Metallization Pattern

During this development, an innovative technique was found for exploring real-time sintering kinetics in a controlled atmosphere. A technologist (Microscopy Research Laboratories, Inc.) was found who was willing to take scanning electron microscope (SEM) video tapes in various atmospheres at high temperatures. The system at Microscopy Research Laboratories is instrumented so that video tapes of real-time processes display pressure, temperature, resolving power, and time. The temperature is controllable to 1600°C, and the pressure to approximately 2 torr. By using a Be window, x-ray analysis with energy dispersive spectroscopy (EDS), or wave dispersive spectroscopy (WDS), is available at temperature. SEM video tapes of selected metallization systems were taken in both air and carbon monoxide and were used to modify the metallization formations for this contract. This technique is being used to study the material science aspects of new metallurgical systems.

Purdue University (Reference 64) investigated the feasibility of using MOD Ag-based inks capable of being screen printed as front contact metallization for solar cells. Generic synthesis procedures were developed for the metallo-organic compounds investigated. The results of this study led to a number of conclusions. Silver neodecanoate was found to be the most suitable MOD component for use in thick-film inks, but the quality of the inks was found to be highly dependent on its purity. Benzene was the most suitable solvent for silver neodecanoate, and tetrahydrofuran was a less desirable alternative. A combination of neodecanoic acid and butyl

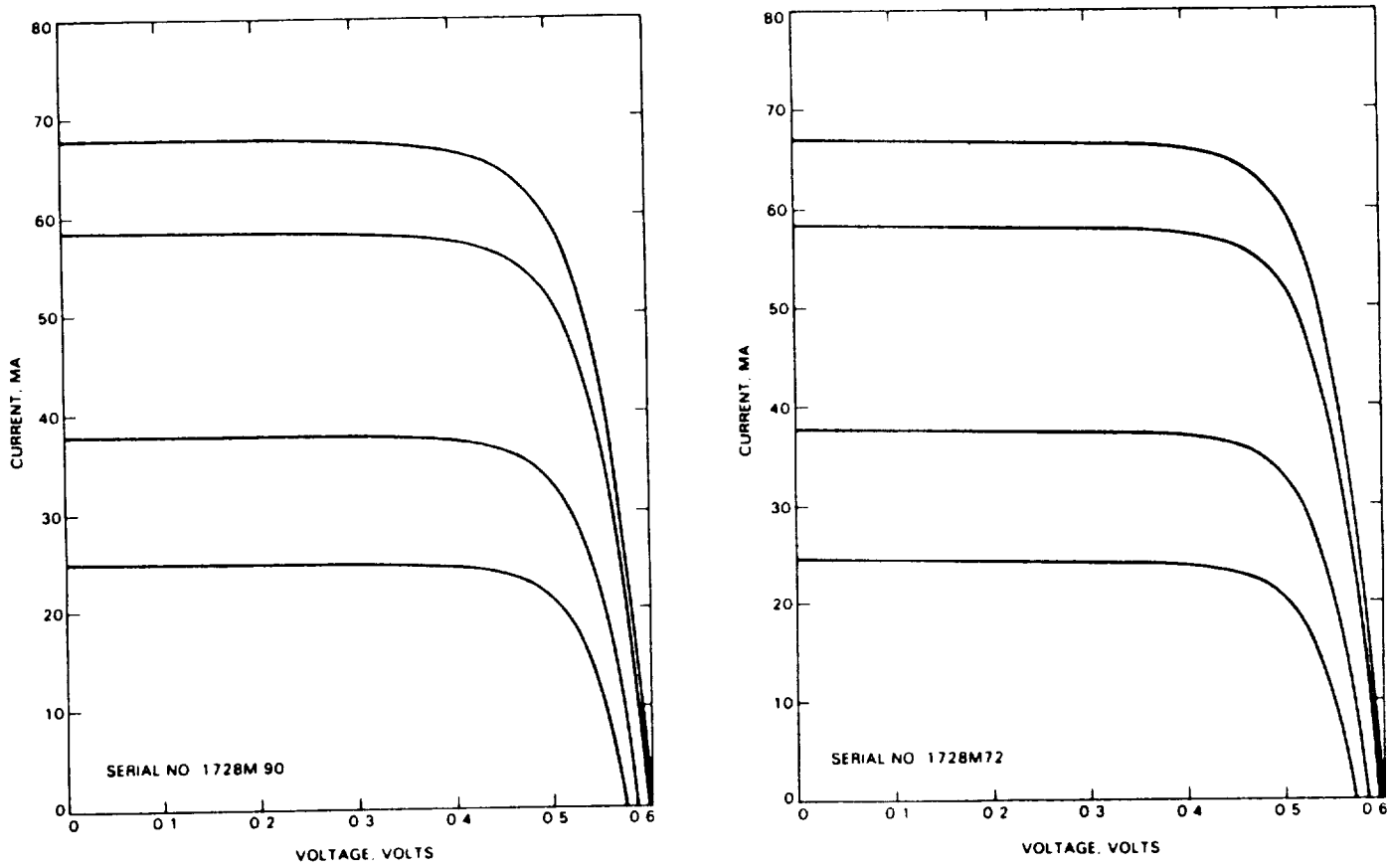


Figure 24. Current-Voltage Characteristics of 1728M-90-Mo/Sn and1728M-72-Ag

carbitol acetate imparted suitable rheology to Ag MOD inks for screen printing. A permanent binding agent was found necessary to obtain reproducible long-term adhesion. Bismuth 2-ethylhexanoate, which decomposes to bismuth oxide upon firing, was found to be suitable for this purpose. The addition of platinum 2-ethylhexanoate imparted solder leach resistance characteristics to the resulting film. Fired films with a metal content of 99% Ag and 1% Bi were the most suitable inks developed for front-metal contacts. However, contact adhesion continued to be a problem when any of the MOD ink formulations were printed directly on silicon. The best cell performances were obtained when the MOD ink formulations were printed on top of evaporated titanium and palladium metal films.

Electrink Inc. of San Diego, California, participated in the investigation of MOD inks by further developing generic fabrication techniques for formulating MOD film compositions. This was a small effort, but was very useful in demonstrating the reproducibility of MOD ink films.

The basic problems encountered above were caused by large-area shadowing inherent in the screen-printing process and the inability to obtain adequate metal conductivity with the thin MOD films. Purdue (Reference 65) developed a method of circumventing these problems by modifying an on-demand ink-jet printing system. The print system itself was modified to accept computer control of the deposition system. The rheology of the inks has been modified, and lines as thin as 50 μm (0.002 in.) and multiple layers (up to five) have been demonstrated.

3. Plating

Historically, silicon solar cells were first produced with plated contacts. The system used was deposition of Ni by electroless methods, followed by solder buildup to provide adequate conductance, and to provide an interconnectable contact area.

Solarex (Reference 66) used this system for low-volume production of terrestrial solar cells. In the referenced contract, they modified their system to handle larger wafers in volume production and to provide an acceptable contact to an A1 screen-printed back contact. Photowatt (Reference 67) modified the above system (to improve adhesion and the ohmic contact) by adding a thin (50 Å) layer of gold, also deposited by electroless methods. They also modified their processes to handle larger wafers in a production environment.

To further improve adhesion and the ohmic contact, a metal plating sequence was developed by Motorola (Reference 68) which allowed selective applications of metal contacts to all exposed silicon on solar cell surfaces. The metallization includes both immersion and electroless Pd plating, heat treatment to form Pd silicide (Pd_2Si), electroless Ni plating, and a subsequent solder coating. The application is selective in that metal is applied, in additive fashion, only to those cell areas on which metal is desired, eliminating the need for any subsequent metal removal or wastage.

As shown in Figure 25, the completed metallization system consists of three layers upon the silicon substrate: a Pd_2Si/Pd first layer, a Ni second layer, and a Pb/Sn solder third layer. Because front and back cell contacts are formed simultaneously, the metal system on the back surface is the same as that on the front surface.

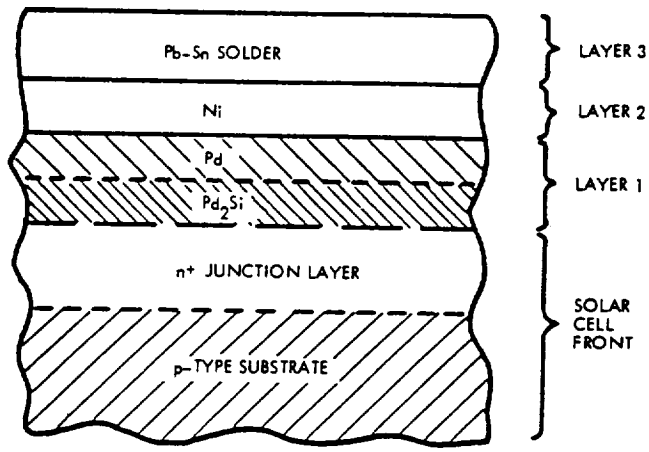


Figure 25. Palladium-Nickel-Solder Metallization System, Shown for Front of a n-on-p Silicon Solar Cell

The first layer of Pd_2Si is formed by heat treating the plated Pd layer. (The Pd may or may not be reacted completely.) The Pd_2Si serves as an adherent, ohmic contact to the silicon. The Pd layer can be heat-treated at moderate temperatures to form the Pd_2Si without fear of rapidly degrading shallow junction solar cell characteristics. The silicide formation is responsible for the excellent adhesion of the metal system. In principle, this layer can be very thin. In practice, the Pd layer has produced the most reliable results when plated to thicknesses (before reaction to form Pd_2Si) between 500 and 1000 Å.

The second layer of Ni provides a solderable metal surface which protects the Pd layer against rapid dissolution in molten Pb/Sn solder. The Ni itself dissolves very slowly in solder. Ni layer thicknesses as great as 5000 Å have been used. Obviously, the longer the Ni layer must withstand molten solder during solder coating and interconnection reflow operations, the thicker this layer must be.

The third layer of Pb/Sn solder provides the required electrical conductivity while still using a low-cost metal. Moreover, solder is known to provide an additional degree of protection against ingressed moisture and contaminants from the terrestrial environment. Typically, 60 Sn/40 Pb solder has been used, although other solders are applicable.

The basic process sequence for applying the Pd/Ni solder metallization system with selective plating techniques is listed below:

(1) Immersion Pd coat (displacement reaction).

(2) Heat treatment (silicide formation).

(3) Scrub (remove loose Pd deposits).

(4) Electroless Pd plate (autocatalytic reaction).

(5) Heat treatment (additional silicide formation).

(6) Electroless Ni plate (autocatalytic reaction).

(7) Solder coat.

Many variations of this process sequence were studied, but the steps listed above have given the most repeatable application of this metal system.

Using the above Pd/Ni solder system as a baseline, new systems were evaluated which showed them to be potentially more cost effective. Motorola (see Reference 68) developed a system that eliminated the use of electroless Pd and substituted Cu for solder as the main conductor. This new system used an electrolytic Ni plating process directly on silicon to allow the formation of a controllable Ni silicide (Ni_2Si) to be used as a diffusion barrier for Cu and prevent degradation of the junction characteristics. Cu was subsequently electroplated to this Ni_2Si layer and acted as the main conductor. Thermal stress tests showed this to be a viable system. Electrically equivalent cells were produced and the economic analysis showed it to be more cost effective than the baseline process.

A parallel study by Applied Solar Energy Corp. (Reference 69) evaluated the technical feasibility and the cost effectiveness of a number of Cu-plated contact systems for high-volume production of low-cost solar array modules. Couples of Cu→Ag, Cu→Be, Cu→Cr, Cr→Cu, Cu→Fe, Cu→Li, Cu→Ni, Cu→Pd, Pd→Cu, Cu→Pt, Cu→Sb, Cu→Ti, Cu→U, and Cu→Zr were investigated. The results of both the literature study and experimentation concluded that Ni was the most viable, cost-effective diffusion barrier for Cu systems.

Based on the cost effectiveness of the copper systems, Westinghouse (see Reference 56) substituted an evaporated TiPd electroplated Cu system for an evaporated TiPd electroplated Ag system. The new metallization system was transferred to the volume dendritic web production facility.

4. Novel Approaches

Novel systems are combinations of the processing technologies described above or are unique processes in themselves.

Illinois Tool Works (Reference 70), whose initial investigations were under the name Edurex Corp., developed and demonstrated metallization systems based on ion-plating technology. Ion plating is a vacuum metallization process where the depositant is evaporated from a source (W filament, e-beam, etc.) into a high-frequency electrical field where the material is ionized and then accelerated by a DC field toward the substrate. This process, shown schematically in Figure 26, combines the high deposition rates associated with physical vapor deposition and improved adhesion without

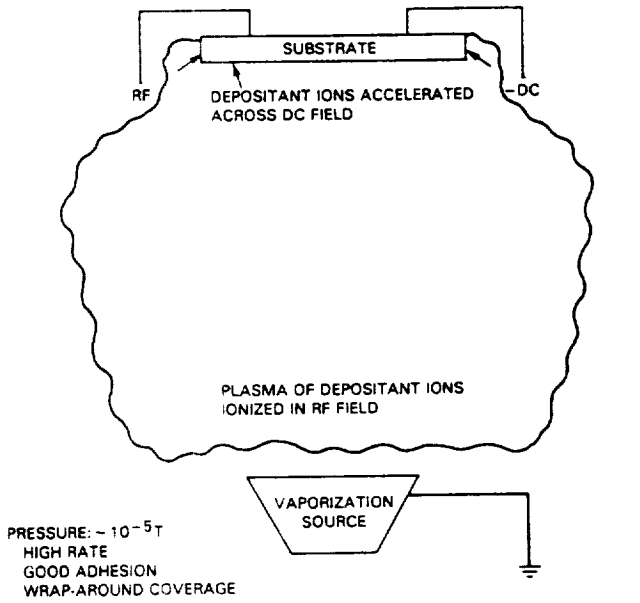


Figure 26. Gasless Ion Plating

the entrapment of Ar gas associated with sputtering. Ag, Al, Ni/Cu, Ti/Cu, and Cr/Cu were successfully deposited on silicon substrates. Cells were fabricated, but the economics of the state-of-the-art technology precluded further volume equipment development.

Caltech (Reference 71) explored the use of diffusion barriers to stabilize metallization systems used to form the contact to the silicon. The difficulty is that the notion of a diffusion barrier is derived from bulk considerations. The time required to penetrate a layer by diffusion decreases with the square of the layer thickness. The diffusivity (in thin films) is typically determined not by bulk diffusion, but by diffusion along extended defects. This diffusion is many orders of magnitude faster than bulk diffusion at the temperatures encountered by the device. The defects in a film are strongly dependent on the conditions prevalent during deposition. For diffusion barrier applications, the fabrication process is as important as the choice of the metal system. This crucial point is often overlooked.

Professor Nicolet, at Caltech, has classified diffusion barriers (according to the mechanism by which they prevent or retard the diffusion process) as passive barriers, sacrificial barriers, or stuffed barriers. A schematic representation, along with examples of each, are shown in Figures 27, 28, and 29. The stuffed barrier derives its low atomic diffusivity to impurities that concentrate along the extended defects of a polycrystalline layer. Sacrificial barriers exploit the fact that some (elemental) thin films react in a laterally uniform and reproducible fashion. When a film reacts in that fashion on both sides, and when the reactions proceed more rapidly than the diffusion through the films, an effective separation is accomplished as long as the film is not totally consumed in the reaction. Passive barriers are those most closely approximating an ideal barrier. This barrier operates because it has a tendency to be chemically inert or nonreactive with

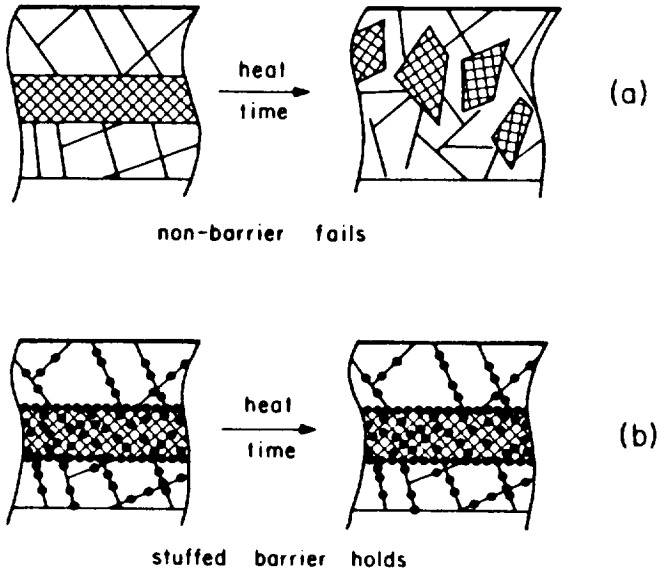


Figure 27. Stuffed Barrier

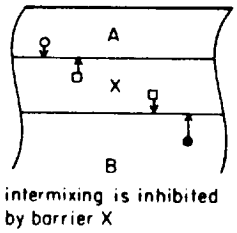


Figure 28. Passive Barrier

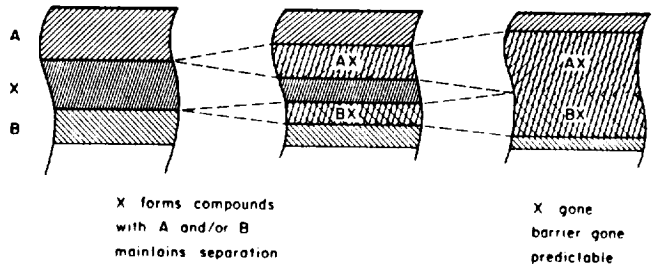


Figure 29. Sacrificial Barrier

the two materials it separates. Barriers capable of withstanding high temperatures (>500 °C) for extended periods of times (>30 min) have been deposited on silicon substrates. These include amorphous films of Ni–W, Ni–N–W, $W_{60}Zr_{40}$, W–N, Ti–N, and W–O applied using sputtering techniques. This is an ongoing investigation.

In the area of novel processing sequences, Spectrolab (References 72 and 73) demonstrated the feasibility of forming solar cell collector grid contacts using the Midfilm (registered trademark of the Ferro Corp., a subcontractor for the program) process. A block diagram of the process sequence is shown in Figure 30, with those involving the Midfilm process highlighted.

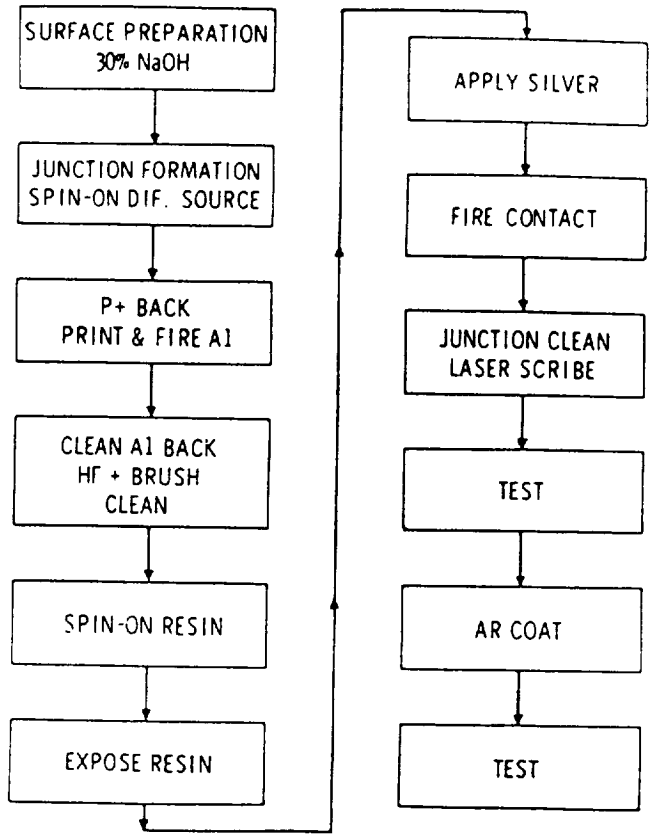


Figure 30. Midfilm Process Sequence

This process has been described as one that attains a line resolution comparable to photoresist methods with a process related to screen printing.

The surface to be processed is first coated with a layer of proprietary (to Ferro) photopolymer material. Upon exposure to ultraviolet (UV) light through a suitable mask, the polymer in the non-patterned area cross-links and becomes hard. The unexposed pattern does not cross-link and remains tacky. The conductor material is applied in the form of a dry mixture of metal and glass frit particles that adhere in the tacky pattern area. This assemblage is then fired to decompose the polymer and sinter the conductor powder. Its analogy to thick-film screen-printed metallization systems is apparent.

Five conductive powder compositions were selected as possible Midfilm metallization candidates. They were:

(1) Fine flake Ag powder (98%), 2% frit (80 PbO, 10 B_2O_3, 10 SiO_2).

(2) Ferro Ag powder (98%), 2% of above frit.

(3) TFS 3347 composition, no screening medium.

(4) Ferro Ag powder (98%), 2% Spectrolab frit.

(5) Ferro Ag powder (98%), 2% Ferro Bi frit.

Cell efficiencies above 14% (AM 1, 28 °C) were achieved with fritted metallization systems [Item (2) was

best]. A feeling for geometry control and finished-sintering characteristics can be obtained from Figure 31 showing both a high magnification cross section and a plan view of a portion of a cell.

The contract reached its objectives and the conclusions were that:

(1) Metal systems used were more reproducible and less expensive than their thick-film counterpart.

(2) Equipment requirements were modest and inexpensive.

(3) This method would be ideally suited for mass production if equipment were developed to handle large-volume production.

Figure 31. Cross Section of Grid Line and Substrate

Photowatt (Reference 74) proposed and investigated a process that consisted of screen printing metal conductive inks over a Si_3N_4 AR coating, followed by electroplating with Cu to reduce grid-line resistance. Ni was the metal of choice for the initial conductor investigations. Later, the work was expanded to include additions of Sn and/or Ag. The plating technique selected was that of didactic (brush) plating and was originally performed by a subcontractor, Vanguard Pacific; later it was transferred to Photowatt.

Electro-Science Laboratories, Inc. (ESL) was chosen as the subcontractor for thick-film ink formulations. Fritted and fritless Ni and fritless Sn-based printing inks were evaluated. The process sequence used is shown in Figure 32.

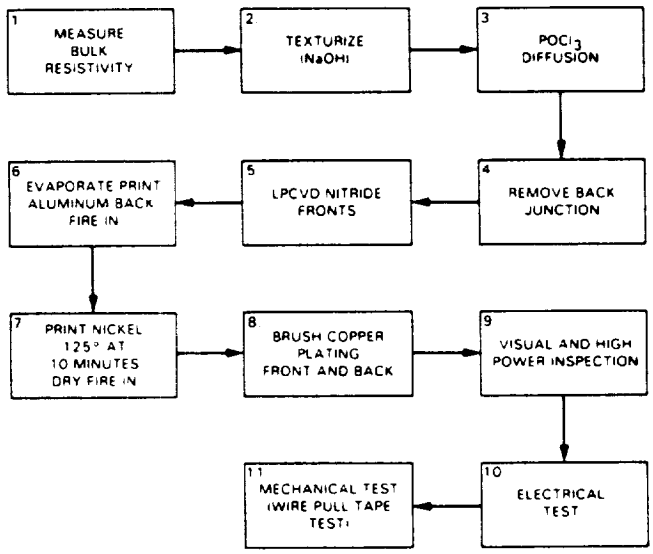


Figure 32. Process Sequence

Although efficiencies as high as 9% were observed with fritted Ni contacts, curve shapes generally were poor, reflecting high series resistance. In addition to high series resistance, problems encountered included the loss of adhesion of the Ni contacts during plating. The Sn-based contacts were quite susceptible to oxidation during firing, and also had inferior curve shapes and poor adhesion. The addition of Ag to the Ni formulations improved the curve shape as shown in Figure 33. However, SEM examination of the paste/Si_3N_4 interface after exposure to Cu plating revealed a prevalence of frit at the interface, with evidence of loose frit residues. A process for firing Ni or Sn-based formulations through a Si_3N_4 AR coating was not developed.

In a parallel program, SOL/LOS (Reference 75) investigated metallization processes based on screenable pastes with Ni as the major conductive component, applied and fired through Si_3N_4-coated wafers. Two commercially available pastes (Thick-Film Systems 5517 and Cermalloy 7028-5) were experimentally evaluated.

To isolate the complex variables introduced by the use of Ni pastes on an Si_3N_4 coating, reference tests were performed with evaporated Ti-N films and with a commercially available Ag-based ink (Du Pont 7095). The experiments with this film Ti-Ni metallization determined the role of the binder in the Ni-based thick-film pastes. The Ag-based system established the difference between Ni and Ag as the contacting metals.

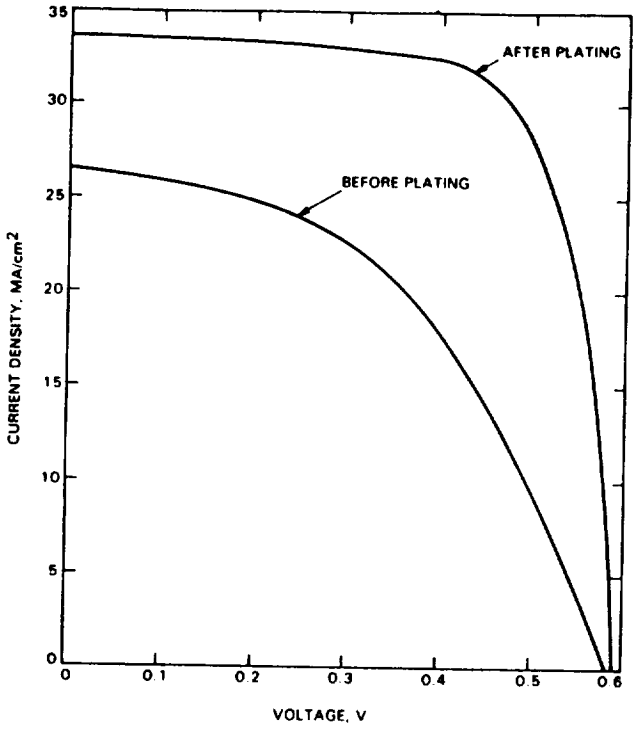


Figure 33. TSF Ni 5517 + 30% EMCA Ag 7069 Fired at 700°C for 5 min

The metallization with the commercial Ni-based systems was not successful in terms of bond strength, solderability, or electrical characteristics. The addition of 10% Du Pont paste 7095 to the Thick-Film System 5517 significantly improved cell characteristics, but was not repeatable enough to warrant further investigation. The contract was completed at the conclusion of this 5-month investigation.

Westinghouse (Reference 76) investigated and developed metallization processing techniques based on the use of a laser as a pyrolytic source. A laser-enhanced plating process was developed using an argon-ion laser, X-Y scanning mirrors, and a Cu plating solution on a silicon substrate coated with evaporated TiPd. A series of 1-cm-long, dense, uniform Cu lines, 25 μm wide and 600 Å thick, were plated with a mirror scan rate of 25 cm/s, a total exposure time of 25 μs, a laser power of 4 W, and a negative plating current of 1 mA. This translates into a dramatically high plating rate of 12 μm/s. No photolithographic or other masking processes were used because the lines plated only where scanned. In a second application using the same argon-ion laser system, MOD films were pyrolytically decomposed on TiPd films, Ti-only films, and on bare silicon. These thin (2000 Å) films of Ag-based compounds were then electroplated to greater than 4 μm to provide the required conductivity. On the TiPd base, devices were produced with efficiencies of greater than 16.6%, which is equivalent to Westinghouse baseline cells. In the case of bare cells, the subsequent plated Ag did not adhere because of stresses induced by the plating.

JPL in-house efforts have been applied to five primary areas:

(1) *Baseline Process Sequence.* This involves providing a laboratory capable of producing cells according to a specific baseline process so that individual processes or process sequences can be compared.

(2) *Developed Process Verification.* This same laboratory is then used to verify the processes developed by the contractors. The method used is to faithfully reproduce the published process specification of the contractor.

(3) *Sensitivity to Process Variables.* In most cases, specific processes rather than process sequences were developed by outside contractors. The synergisms involved with inserting these individual processes into a sequence were investigated at JPL.

(4) *Economic Verification.* The individual Format A's and the rationale behind their extension to volume production was studied in detail. The Format A input data were used to generate SAMICS computer runs to verify the economics of the process (in some cases at multiple output levels).

(5) *Technology Transfer.* JPL was used as the centroid in transferring these developed cost-effective processes to industry.

D. RELIABILITY

As might be expected, most systems have not been in service long enough nor have they been stress-tested in volume to determine their reliability. The new thrust to high efficiency, however, has reintroduced the space-qualified, very reliable TiPdAg systems for terrestrial use. The only other volume systems out in the field are those using thick-film, screen-printed, Ag-based metallizations. These have not been in the field long enough to determine their reliability level.

E. ECONOMICS

The JPL PA&I Group has been analyzing process-sequence costs since the program's inception. An article on the "Economics Implications of Current Systems" (Reference 77) is worth discussing because it analyzes and updates all the metallization systems. Most of the data for the cost estimates came from Project contractors. The IPEG II methodology (Reference 78) was used to make the cost estimates. Data for the cell performance calculations were taken from a report by M. Wolf (Reference 79) and are used with a grid optimization model (References 80 and 81) developed at JPL.

For each process studied, a maximum metallization thickness and a minimum fine-line grid width were chosen to be consistent with that specific process technology. The cell performance was calculated with

only the metallization bus-bars for current collection and again for cells having a fine copper ribbon fastened over the metallized bus-bar pattern. These costs are shown in Tables 3 and 4.

Table 3. Cost Breakdown, No Strapping, $/m^2 (See Reference 78)

Process/System	C(1) (Equipment)	(109) (sq ft)	(2.1) (Direct Labor)	(1.2) (Materials) + 1.2 (Utilities)	Total
Evaporation, State of the Art (SOA)	7.35	2.42	32.40	50.50	92.7
Evaporation, Advanced	5.26	0.98	4.25	3.61	14.1
Print, Ag, SOA	0.71	0.30	0.52	5.09-25.07	6.6-26.6
Print, Ag, Advanced	0.35	0.15	0.26	6.82-33.91	7.6-34.7
Print, Al, SOA	0.71	0.30	0.52	0.21	1.7
Print, Al, Advanced	0.35	0.15	0.26	0.20	1.0
Print, Mo-Sn	0.35	0.15	0.26	1.20-2.20	2.0-3.0
Electroless, Ni-Solder, SOA	1.43	1.89	2.45	1.93	7.7
Electroless, Ni-Cu, SOA	1.61	1.69	2.02	1.34	6.7
Electroless, Ni-Cu, Advanced	1.35	1.75	3.35	2.15	8.6
Midfilm, Ag	0.20	0.29	0.38	5.55-25.84	6.4-26.7
Midfilm, Mo-Sn	0.20	0.29	0.38	1.53-2.52	2.4-3.4
Ion Plating, Ti-Ni-Cu	NA	NA	NA	NA	6.0

Table 4. Change in Cost Because of Strapping, $/m^2

Process/System	New 1.2 (Materials + Utilities)	Plus Strapping	New Total
Evaporation, SOA	48.68	1.0	91.8
Evaporation, Advanced	3.60	1.0	15.1
Print, Ag, SOA	2.65-12.88	1.0	5.2-15.4
Print, Ag, Advanced	3.94-19.52	1.0	5.7-21.3
Print, Al, SOA	0.14	1.0	2.7
Print, Al, Advanced	0.11	1.0	1.9
Print, Mo-Sn	0.47-0.85	1.0	2.2-2.0
Electroless, Ni-Solder, SOA	1.63	1.0	3.4
Electroless, Ni-Cu, SOA	1.33	1.0	7.0
Electroless, Ni-Cu, Advanced	2.14	1.0	9.6
Midfilm, Ag	2.85-12.37	1.0	4.7-14.2
Midfilm, Mo-Sn	0.87-1.23	1.0	2.7-3.1
Ion Plating, Ti-Ni-Cu	NA	1.0	7.0

The process cost versus process performance level (assuming a lossless cell with no resistance or shadow losses) for state-of-the-art and advanced systems concepts is shown in Figure 34. This defined an efficient frontier; a point is said to be on the efficient frontier if there is no other point that has both a higher performance ratio and a lower cost. This figure shows the relationships of the metallization systems described above.

F. KEY ACCOMPLISHMENTS

Improvements in metallization systems have been detailed in the previous discussions. A list of the key accomplishments with the associated contractor(s) credited is given below:

(1) Thick-film screenable cost-effective metallization processes using Ag, Al, AgAl, Cu, and MOD AgBi (Spectrolab, B. Ross Associates, RCA, Purdue University, Electrink, and SOL/LOS).

(2) MOD films using low-temperature processes, $< 390^{\circ}$ (Purdue University, Electrink, and Westinghouse).

(3) Reliable plating systems using Pd and Ni followed by solder buildup by immersion or by Cu plating (Motorola, ASEC, Solarex, and Photowatt).

(4) Pyrolytic decomposition of MOD films using a laser as the thermal source (Westinghouse).

(5) Development of a generic fabrication process for producing MOD films and transferring the technology to industry (Purdue University and Electrink).

(6) Diffusion barriers for high reliability (Caltech).

G. CURRENT STATUS

Although Project milestones on costs, performance, and production rates were demonstrated in small quantities for metallization processes, they are not being verified by pilot production runs because of Program redirection.

H. REQUIRED FUTURE TECHNICAL NEEDS

Studies to date have emphasized the emerging importance of materials science in understanding the synergistic processes occurring during contact formation. This leads to two basic requirements:

(1) Studies of material interactions in basic metallization processes should be continued if the 30-year reliability goals of the Project are to be realized.

(2) MOD film formulations and MOD film adhesion directly to silicon, with no intermediate metal films, should continue to be investigated.

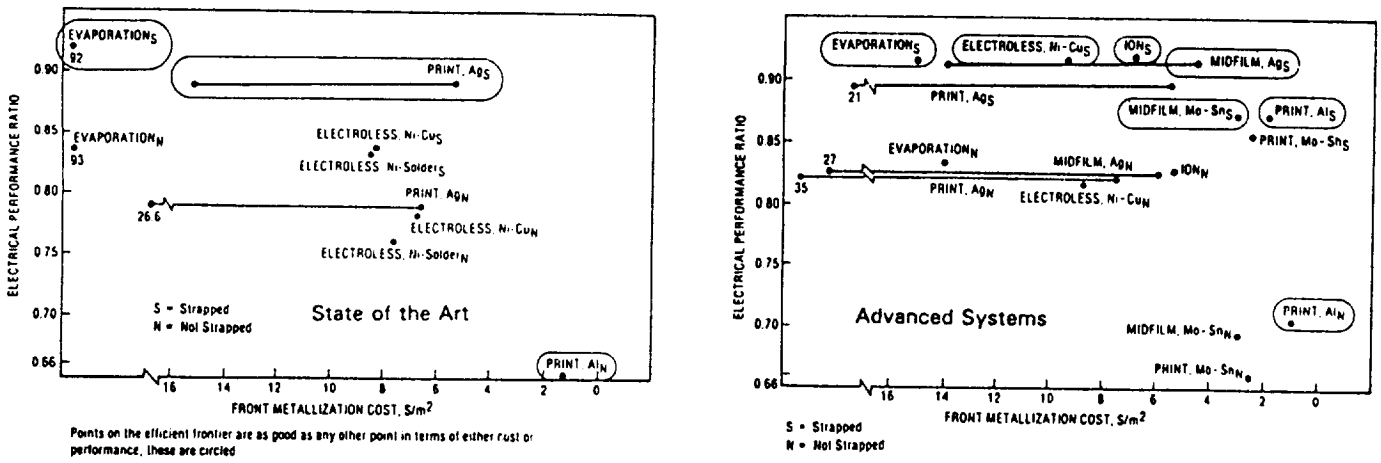


Figure 34. Combined Efficient Frontier

SECTION V

Module Fabrication

A. BACKGROUND

Assembly processes in 1975 were a true reflection of the cost and intended function of terrestrial PV modules. With prices in the range of $\$40/W_p$ (1975 dollars), the only economic use for PV power was for remote, rugged, or stand-alone systems. Telecommunication repeater stations, ocean buoys, and remote instrumentation installations demanded reliable, maintenance-free systems.

Assembly labor and material costs were approximately $\$3/W_p$ in 1975. Three factors were responsible for these costs: labor-intensive processes, high material costs, and low cell-packing factors. The focus of the assembly process efforts from 1976 to 1986 was to reduce labor and material costs and improve packing factors.

One notable feature of assembly processes was their interaction with a number of other technical areas and FSA Project concerns. Cell interconnection requires a study of interconnect reliability, redundancy, and fatigue failure. Lay-up and lamination required materials that were not commercially available. Cell processing was an obvious concern because the assembly equipment and processes must be compatible with the cells. Block buys, made to encourage industry productivity, created module environmental specifications that had to be met. Large-area, glass superstrate modules triggered studies on the effects of hail, iron content in glass, and design of glass structural panels. All of these efforts were handled by other task groups in the FSA Project such as reliability, block buys, engineering sciences, and encapsulation. The remaining assembly problems were significant, and efforts toward their solution are detailed below.

B. THEORY

Assembly processes do not have a unique, underlying theoretical structure. Each process can be completed in a number of different ways with different process and equipment requirements. Because of this limited content and high diversity, any theory that is involved is included in each process as required.

C. DESCRIPTION OF 1975 ASSEMBLY PROCESSES

Present industry PV module assemblies (Figure 35) are used as models for discussing assembly process developments. This approach is chosen because nearly all of the present processes were developed or actively encouraged by the FSA Project.

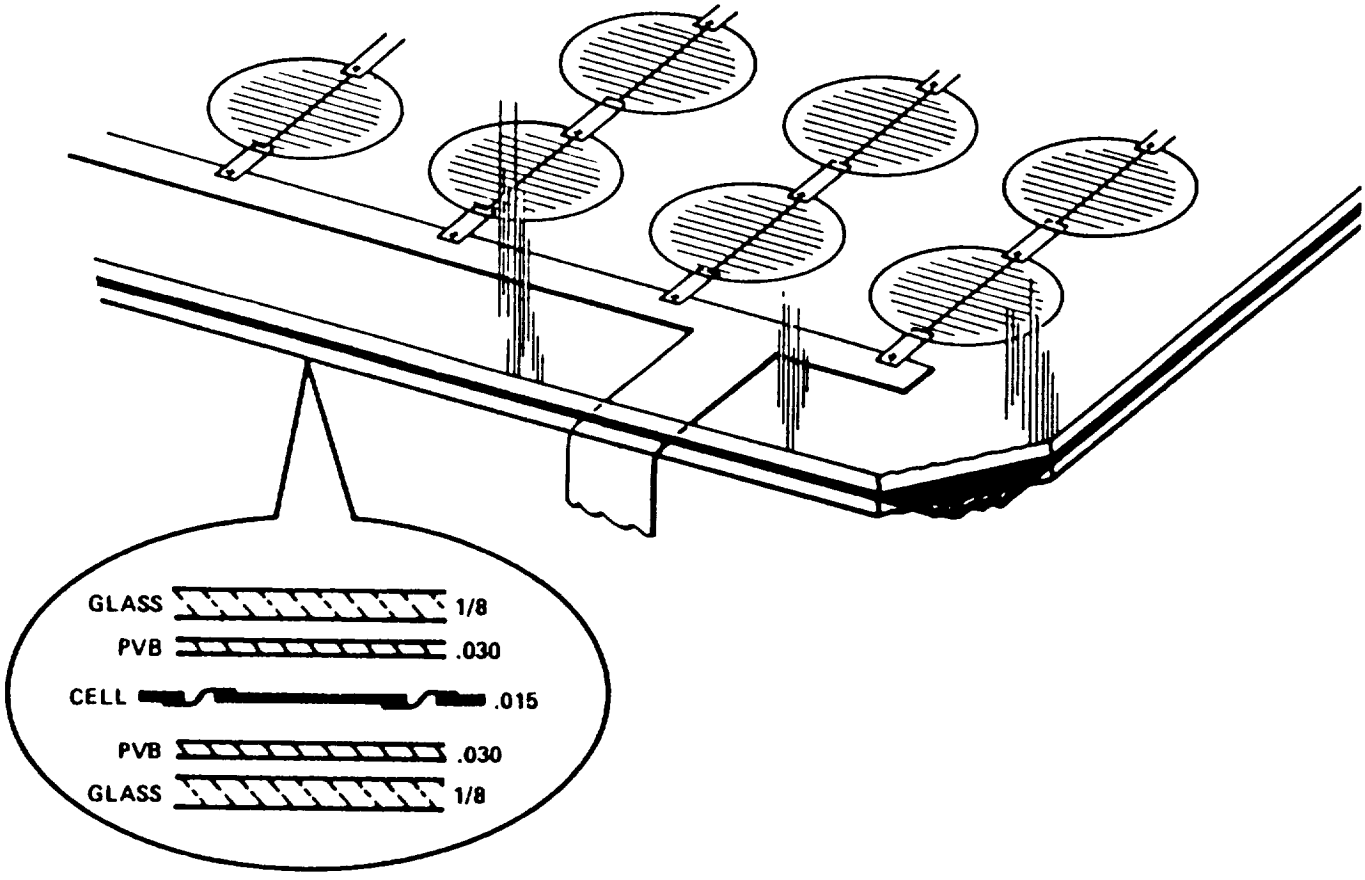


Figure 35. Solar Panel Configuration

Two separate product streams (module assembly and glass superstrates) are of interest in assembly (Figure 36). Module assembly consists of cell interconnection, cleaning, lay-up and wiring, lamination, framing, diode and terminal installation, and testing and packaging. Glass superstrate preparation consists of cleaning, AR coating, and priming. Module assembly processes will be discussed below.

1. Cell Interconnection

Cell interconnection requires attachment of a metal strip from the bottom of one PV cell to the top of an adjacent cell (see Figure 35). Connecting cells together in this fashion creates a series string, much like stacking "D" cell batteries one on top of another. A series string is an ideal method of obtaining high voltage and low current in a module. Unfortunately, one broken cell or interconnect in a series string can cause an open circuit. The preferred circuit for a large module is usually series-parallel with 10 to 15 cells in series in each of 8 to 20 parallel strings (Figure 37). A series-parallel circuit reduces the "hot spot" problem, but does not avoid it entirely. This subject is discussed in more detail in Vol. VI, Engineering Sciences and Reliability.

In 1975, the cell interconnection process involved manual soldering. Hand soldering requires low capital investment and can easily be used to assemble a variety of special purpose modules. Hand soldering is very labor intensive, however, and requires a robust cell junction and adherent metallization.

2. Cleaning

A string of interconnected cells is very fragile and awkward to handle. If solder flux or any other contaminant has been deposited on the cells, it must be removed. Contaminants can affect module life by degrading adhesion or creating corrosion problems. Most cell string cleaning involved using cotton-tipped swabs and solvents to remove visible contaminants. If the cell strings were short, they might be placed in an ultrasonic cleaning tank.

3. Lay-up and Wiring

A variety of fixtures, tapes, and substrates was used to assist in the location of cell strings to form a module. Connecting cell strings together to form the desired module circuit required additional hand soldering and more cleaning. At this step, wire leads or feed-throughs were also attached to provide connection to the interior of the module.

4. Lamination

A lamination process was not available to assemble modules in 1975. The bulk of the production modules was encapsulated by use of a silicone or epoxy potting compound. These modules were very resistant to the environment; however, there were other problems. Silicones are expensive, and a typical module might have a 3/8-in.-thick layer of silicone pottant (high usage of a high-cost material). Potting with silicones was a "dirty" operation and had to be kept segregated to avoid contaminating the cell fabrication line with silicones. Silicone surfaces are also very hard to clean once they have been exposed to dirt accumulation.

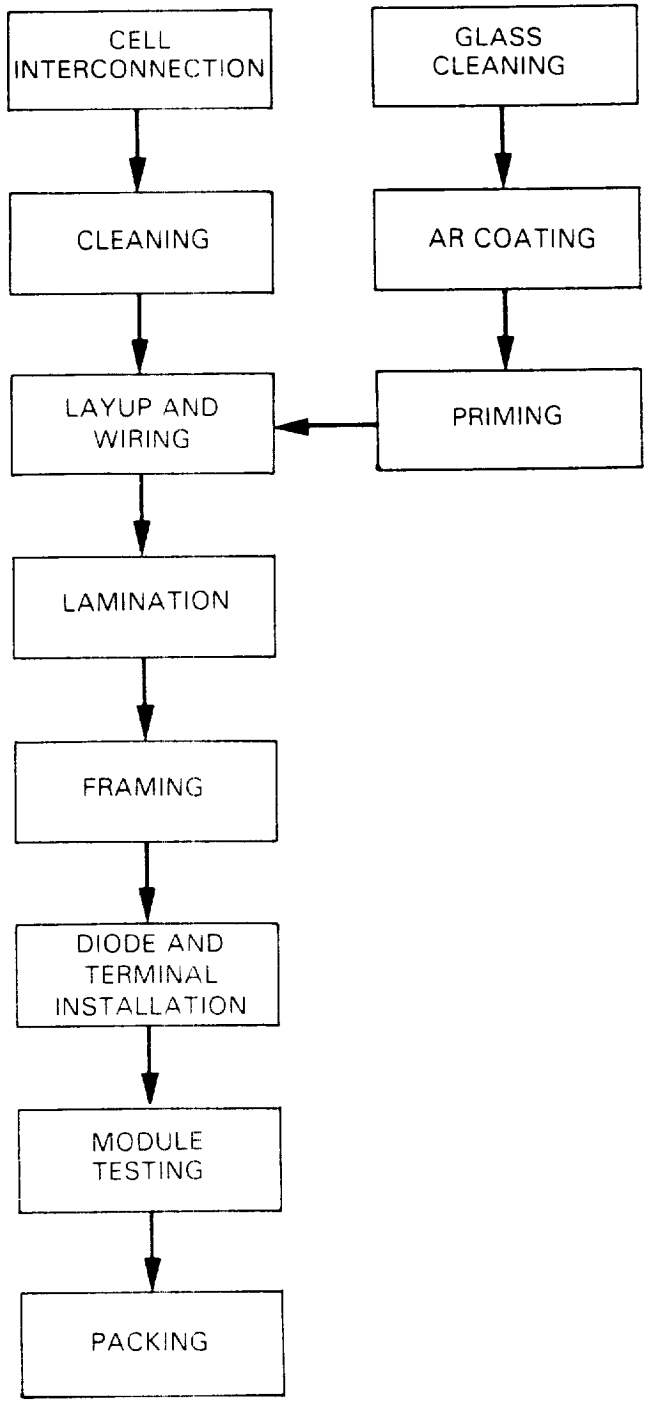


Figure 36. Assembly Process Sequence

5. Framing

Most module frames were made out of extruded aluminum channels much like they are today. Along with the aluminum side pieces, there was often a fiberglass substrate and sometimes a glass cover plate. If there was a cover plate, the silicone pottant would be poured into the box-like module to encapsulate the cells and wiring. If

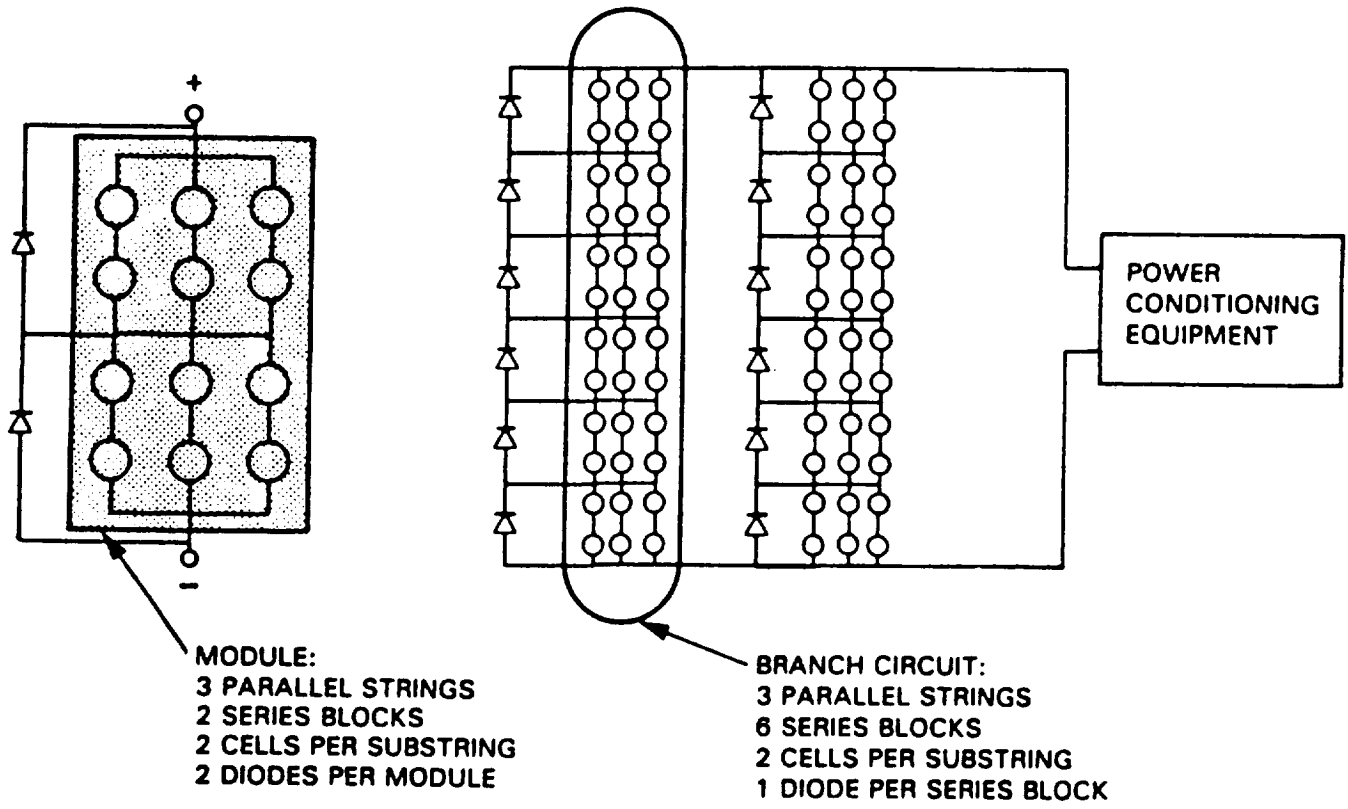


Figure 37. Series-Parallel Nomenclature

there was no cover plate, the silicone was just poured over the cells and substrate.

6. Diode and Terminal Installation

Placement of a bypass diode (if used) occurred after framing or before encapsulation. If the diode required a heat sink (which was the usual case), the diode would be attached to a frame member or placed in a junction box attached to the frame. Terminals or pigtail leads would also be attached to the junction box. Use of a junction box was usually required for a residential installation because of electrical code restrictions.

7. Testing and Packaging

These two process steps were never addressed by the Process Development Area. It was felt that there was limited potential for cost reduction.

D. PROCESS DEVELOPMENT

Process developments will be discussed with a historical rather than process sequential frame of reference. In this way, the contributions from many contractors over a long time period can be kept in context.

1. Phase I

During the Assessment Phase, the three major contractors were all trying to evaluate present solar cell practices and project technology development needs. There were great expectations of rapid market growth from PV cost reductions and high petroleum prices. Final reports from the three contractors (References 82 through 84) reflected state-of-the-art process technology.

Highlights of the final reports are:

(1) Cell interconnection should be automated by use of a rotary table and either parallel gap welding, ultrasonic bonding, or solder reflow.

(2) Copper-clad Invar interconnects should be used to reduce thermal stresses.

(3) Robotic handling of cell strings was proposed.

(4) Laminated modules with cells sandwiched between glass was proposed for best environmental resistance.

(5) Porcelainized steel was suggested as a low-cost module material.

(6) Computer control and data logging in the manufacturing sequence was introduced.

(7) Use of test patterns to monitor processing was urged on an in-line, continuous basis.

Some module design and fabrication suggestions were also made. Two different module designs were proposed: double-glass lamination (as shown in Figure 35) and adhesives (as shown in Figure 38). An edge sealant or foil tape was suggested for the laminated module, and the adhesive module used a compression seal.

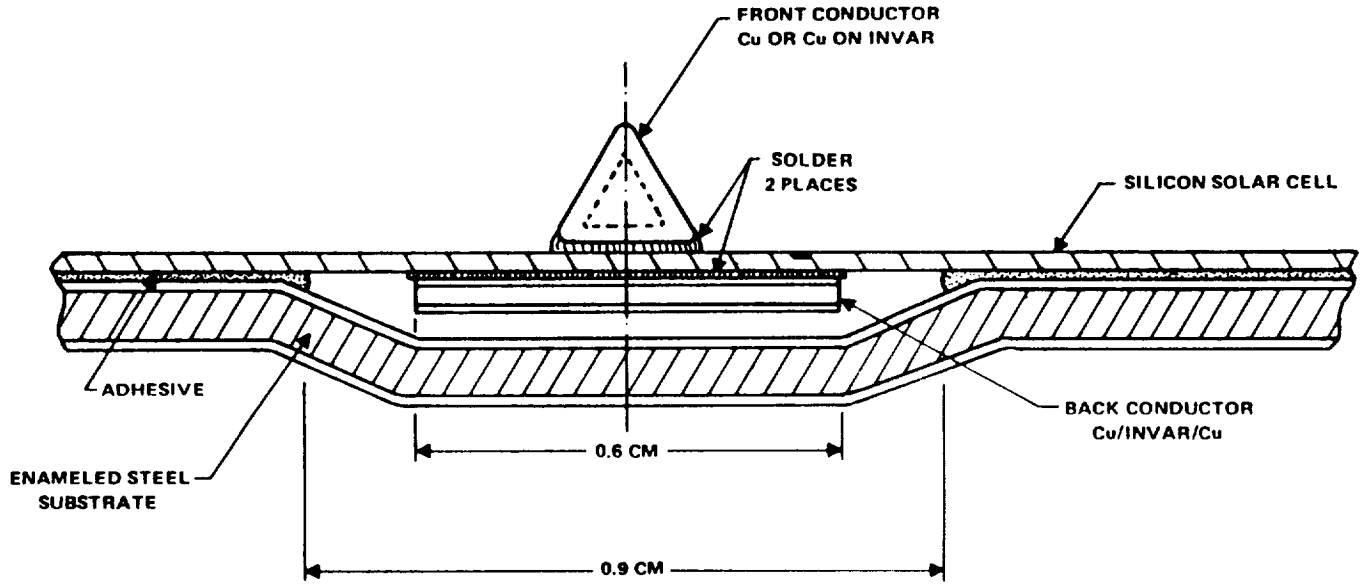


Figure 38. Back Conductor Arrangement of Proposed Large-Scale Solar Array Module

All of the contractors agreed that the $0.50/W goal was feasible given the projected silicon material price goals. Unfortunately, attempts to compare estimates of industry process and material costs between contractors were inconclusive. Each contractor had a different overhead structure. This comparison problem led to early development of the SAMICS, a joint effort between the Process Development Area and the PA&I Area.

2. Phase II

The Process Development Phase was implemented in two stages. The first stage was concerned with development of single processes or module design studies. After sufficient data were gathered, the second stage efforts were focused upon tying well characterized processes together into process sequences. Additional funds were made available from the Tsongas Amendment, which directed the FSA Project to fund contracts leading to near-term cost reductions.

Module development contracts were an integral part of the "Block Buy" effort. Large quantities of state-of-the-art modules were bought from various vendors by the Block Buy Group. This effort forced the industry to develop improved module designs to meet more and more stringent mechanical and performance specifications. The Process Development Area contribution to industry improvement was to fund the more innovative designs that industry wanted to try before committing to a volume order. Contracts in this category were let to Spire Corp.; General Electric; Lockheed Missiles & Space Co., Inc.; Xerox Electro-Optical Systems; Motorola, Inc.; Westinghouse R&D Center; and Solarex Corp.

One innovative approach was the use of electrostatic bonding to attach a glass cover plate to the PV cells and interconnects. Spire Corp. (Reference 85) pioneered this effort which had the appeal of a long life, hermetically sealed module (Figure 39). Very stable electrostatically bonded modules were fabricated.

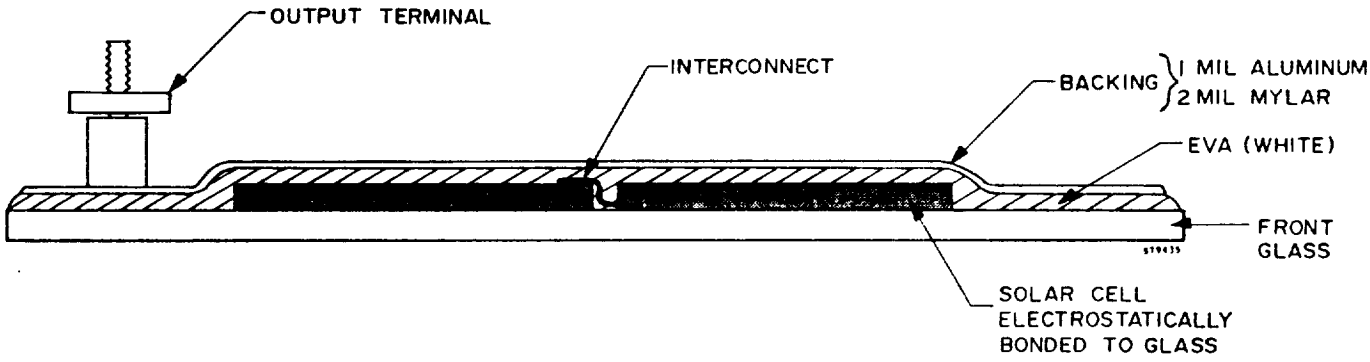


Figure 39. Cross-Sectional View of Integral Front, Electrostatically Bonded Module Assembly

Unfortunately, attempts to scale up the process and reduce its cost were unsuccessful.

The General Electric module concept (Reference 86) was to use the PV modules as roofing shingles. Each module contained a hexagonal PV portion and a rectangular portion for roof attachment and module interconnection (Figure 40). These modules had a built-in economic advantage in that they could be used in place of standard roofing materials. During the period of the contract, it was noted that the cells were more efficient when assembled into a module. Examination showed that light reflected from the white backing material would also reflect from the inside of the cover glass. This second reflection would often return the light to a cell area rather than a cell-to-cell space. The "zero depth concentrator" effect was a serendipitous result.

Lockheed Missiles & Space Co. explored the concept of transparent modules (Reference 87). Allowing light that does not strike a cell to pass through the module should lower the module operating temperature. Lower temperatures result in higher efficiencies. The modules that were fabricated highlighted some problem areas. Silicone primers were ineffective in improving adhesion. More work was needed on mass production assembly concepts such as optical cell orientation, improved cell bonding or film lamination, and improved, nonabsorptive materials. Cell handling and interconnection also had to be improved.

Xerox proposed to assemble cells into a module by mechanical means (Reference 88). A number of different materials and attachment methods were examined and a successful module was constructed. The mechanical attachment approach always raised the question of stress-induced cell cracks. This problem, along with an awkward electrical wiring situation, stopped any future efforts in this area.

A Motorola, Inc. module contract (Reference 89) uncovered a need for more work on multiple interconnects and interconnect stresses. Numerous cell cracks were traced to module flexing and thermal cycling. Reduction of cell and interconnect stress levels became a major Project design goal.

Another module contract with Motorola, Inc. (Reference 90) examined the feasibility of applying AR coatings to glass superstrates. Three methods were considered: acid etching, plasma etching, and acid development of a sodium silicate film. Acid etching gave the best transmission, and the sodium silicate film was the most durable. Plasma-etched films were water soluble and, thus, were disqualified. Control of the acid etching process was a problem along with the large-scale application of sodium silicate.

A study of cell interconnection methods was done by the Westinghouse R&D Center (Reference 91). The methods investigated were: conductive adhesive bonding, parallel gap welding, laser welding, thermocom-

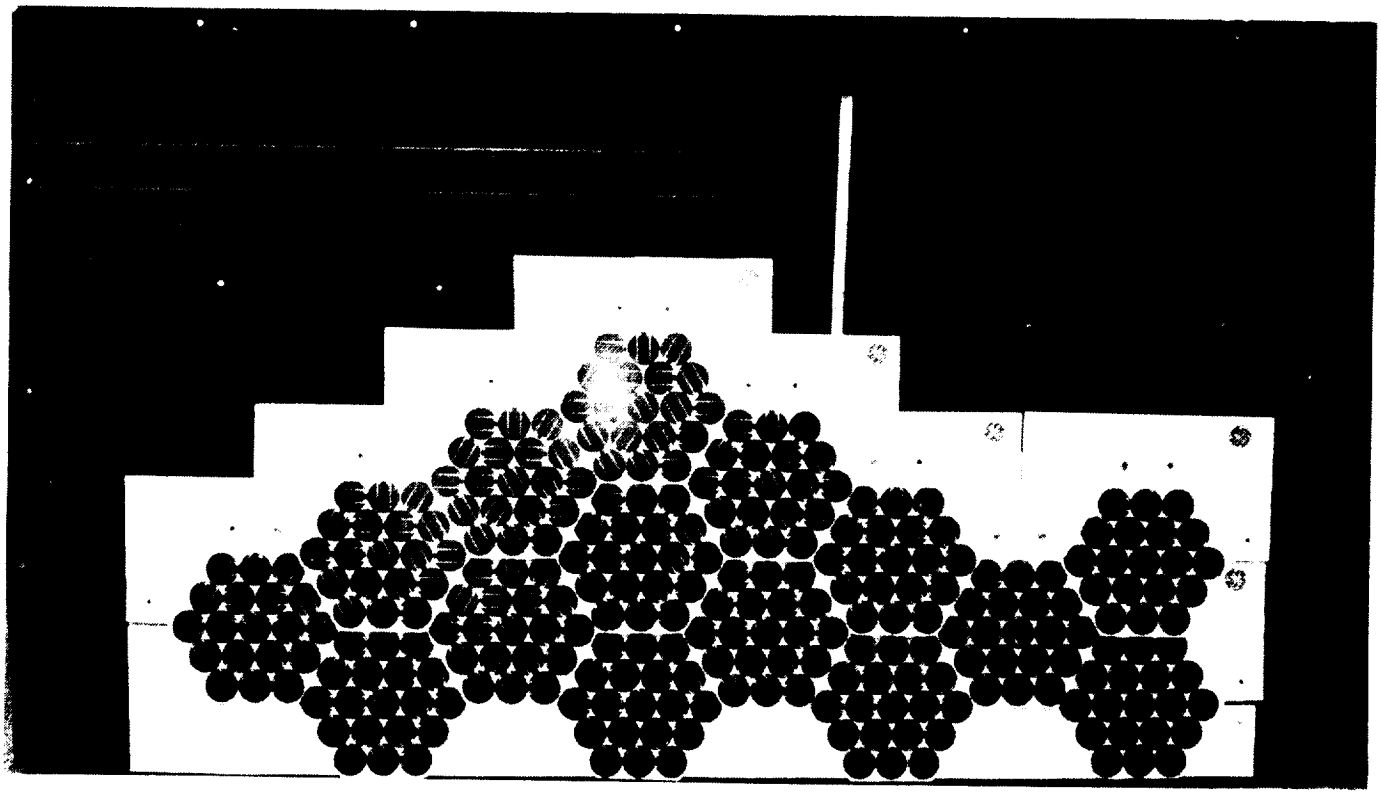


Figure 40. Arrangement of Modules on Simulated Roof Structure

pression bonding, soldering, solder reflow, and ultrasonic bonding. Ultrasonic bonding was chosen for more detailed analysis for several reasons: (1) most materials capable of being bonded, (2) low contact resistance possible, (3) strong bonds achievable, (4) corrosive flux not used, (5) minimum cell thickness buildup (e.g., no solder), (6) moderate capital cost, and (7) low-energy consumption and amenable to automation. Successful ultrasonic bonding was demonstrated; however, BSF created a stressed brittle condition that caused numerous failures. Demonstration modules were fabricated (Figure 41) using a generic silicone molding compound (RTV) as an adhesive/encapsulant, a phenolic backboard, and soldered interconnections.

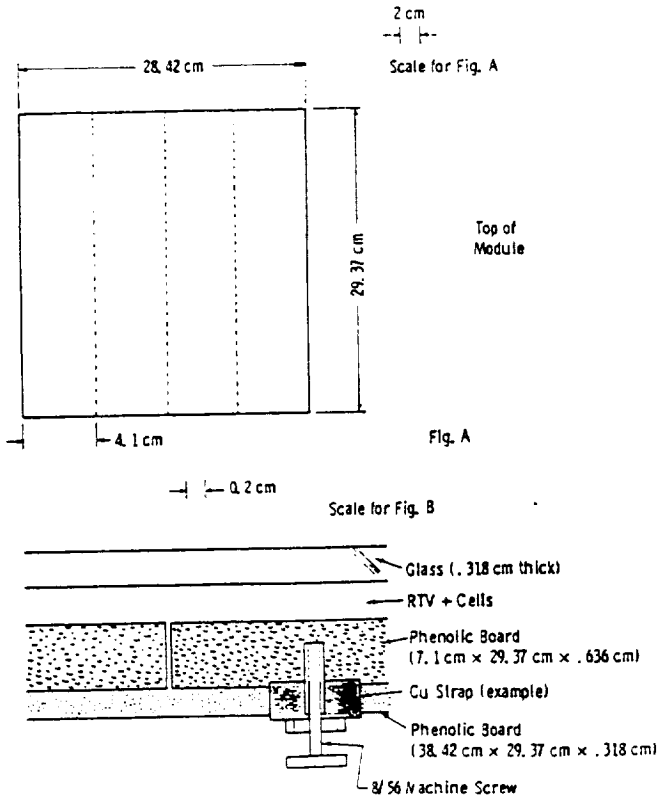


Figure 41. Demonstration Module Design

Solarex Corp. significantly improved module efficiency by use of square cells (Reference 92). Packing factors for modules based on round cells are typically around 70%. Use of square or rectangular cells can improve the packing factor to around 90%. Higher module efficiencies result in less use of module materials and reduced balance of system costs for array structure, land, and array wiring. Any square cells produced at this time must be cut from round wafers with a loss of silicon sheet material. Figure 42 shows a more economical compromise: the semi-square cell.

Additional Phase II efforts concentrated on pushing the state of the art. Five contractors were involved in a variety of activities. Texas Instruments built upon their Phase I experience and investigated the use of a large

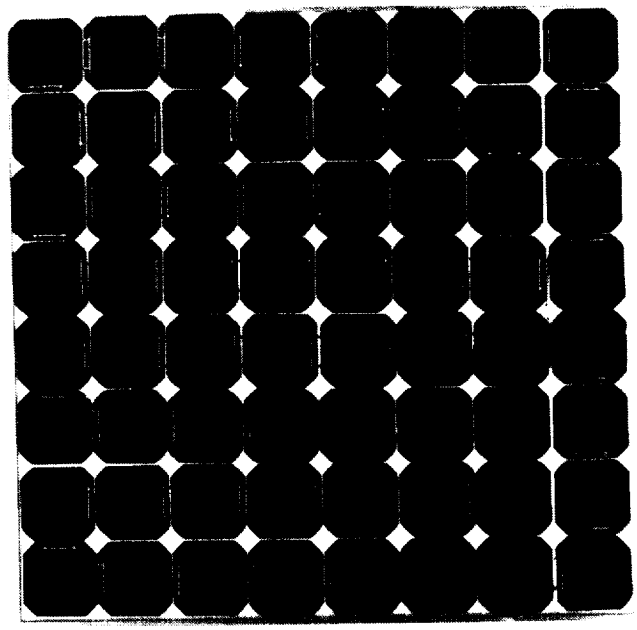


Figure 42. Commercial High-Density Panel

(38.44 cm^2) high-efficiency, tandem junction cell (Reference 93). These cells required more attention to interconnection because each cell was essentially two cells stacked one upon the other. Copper-clad Invar interconnects were developed along with IR reflow soldering. All connections were made on the back of the cells, which reduced shadow losses.

MBAssociates did a study contract on the automation of a cell and module fabrication line (Reference 94). An important part of this study was the extensive use of the SAMICS costing methodology. Soft automation techniques (software driven) and a robot were used as much as possible to allow rapid and inexpensive process equipment changes. Automated cell interconnection is shown in Figure 43. This cell string fabrication machine was built and demonstrated the feasibility of automation. Similarly, an automated module lamination machine, an automated framing station, and an automated edge sealant machine were successfully demonstrated.

Module fabrication cost per watt depends upon more than just module labor and material costs. The importance of higher packing factors has already been discussed; however, mechanical yield is also an important issue. If cells break or have metallization debonding because of assembly processes, then rework and repair costs will increase. Cell failure after lamination is especially serious because the whole module may have to be rejected. The next series of contracts covered these issues and continued the fostering of PV industry technology.

Mobil Tyco (now Mobil Solar Energy Corp.) had developed the EFG silicon sheet process on other FSA contracts. Cells made from EFG substrates were fabricated into modules to demonstrate the feasibility of this new ribbon growth technology (Reference 95). Each

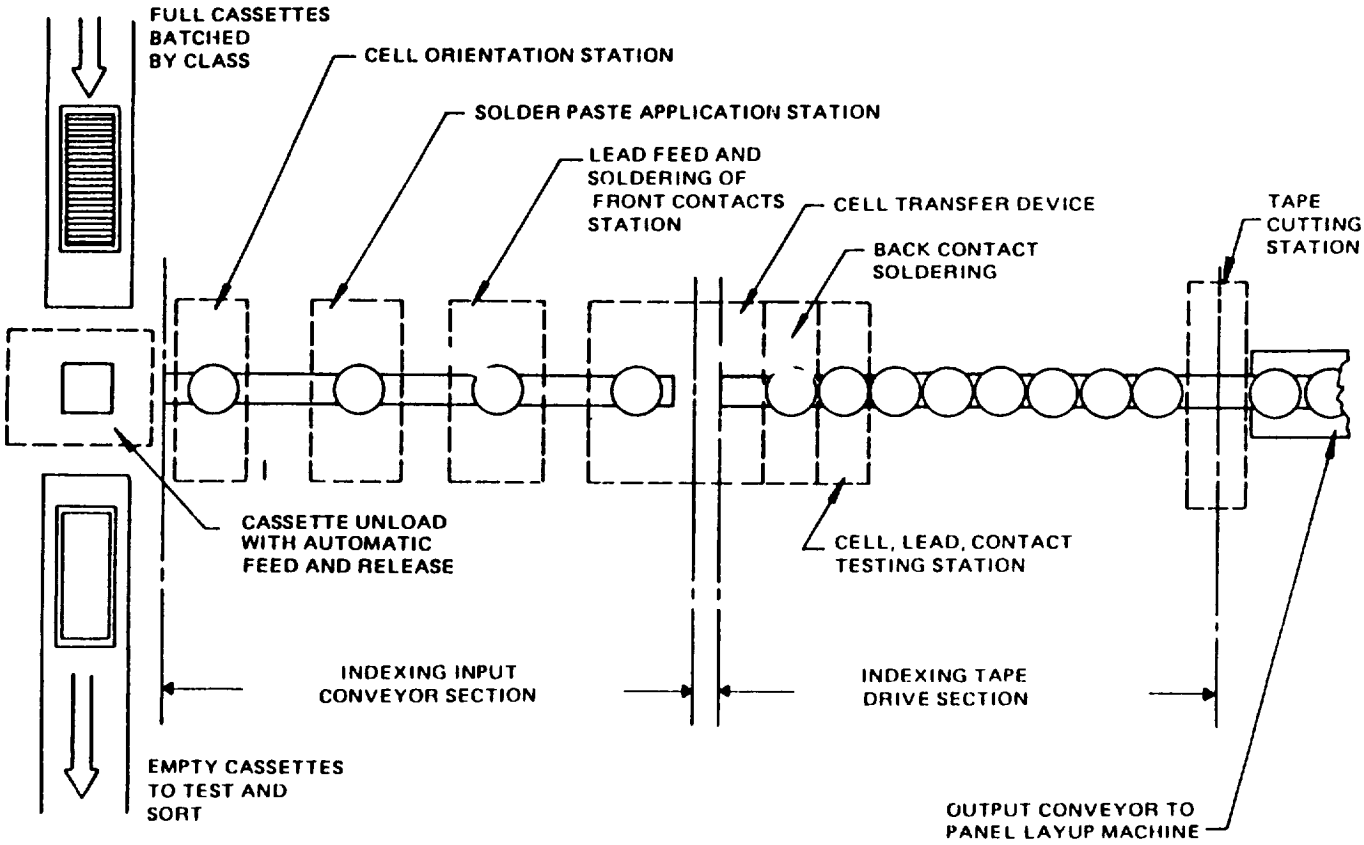


Figure 43. Ribbon Fabrication Machine

module contained 180 each of the 2.5 x 10 cm EFG cells connected with an expanded copper mesh for stress reduction. A high packing factor was achieved by "shingling" the cells to reduce intercell spacing. Because EFG ribbon is a polycrystalline substrate, there was some initial concern about increased handling damage compared to single-crystal Cz substrates. Square cell corners were also considered to be a potential problem. Although these problems were experienced during the contract period, it was concluded that they were tractable with a little care and some special material handling fixtures.

Cell thickness was another mechanical yield concern. There was an FSA research effort trying to reduce silicon substrate thickness. Solarex Corp. evaluated the use of a new multiple-loop sawing technology to fabricate thin Cz wafers (Reference 96). An analysis was made of the effects of wire diameter and abrasive size on surface damage to the wafer. Thin wafers caused no assembly handling problems. The wire saw was much more labor intensive than expected, and a broken wire created wafering problems. A new module design was also explored. The cells were mounted on a substrate and covered with a transparent elastomer. An analysis was made of the effect of hailstone impact on the embedded cells. The analysis showed that a substrate design was feasible.

Optical Coating Laboratory, Inc. (now Applied Solar Energy Corp.) was one of only two space-qualified PV array manufacturers. They were capable of producing small, high-efficiency PV cells, but at a high cost because of space quality assurance constraints. Their contract was to develop a module with an efficiency of 14% (Reference 97). A 14% module requires a 16.5% efficient cell to allow for encapsulation and packing factor losses. Most of the contract effort was spent in achieving 3-in.-diameter cells with an average efficiency of 13.8%. The resultant modules had an average efficiency of 10.9%, which was the highest performance to date of a terrestrial module. Estimated module labor costs were reduced by use of special purpose assembly equipment and jigs.

There was still a need for demonstration of full automation of module assembly by the PV industry. Near-term cost reduction efforts were centered on two major efforts at ARCO Solar, Inc., and Kulicke and Soffa Industries, Inc. The ARCO Solar effort included two major tasks: automated cell stringing and automated lamination (Reference 98). This 2-year program had four milestones: (1) design a module for automated assembly, (2) design and develop prototype automated equipment for interconnection and lamination, (3) operate a pilot line using prototype equipment, and (4) perform a cost analysis. The module design was conventional except for the use of lamination.

A prototype cell stringer was built which used radio frequency (RF) heating to bond the interconnects/bus bars to the top and bottom of a cell simultaneously. Cell metallization did not include the usual wide bus

bar attaching all of the grid lines together. Instead, solder pads on each grid line were connected using a 0.100-in.-wide by 0.003-in.-thick solder-plated copper strip. Over 2,000,000 cells were connected with this prototype or its later modifications which used IR heating instead of RF. Solder flux was removed using an in-line vapor degreaser, ultrasonic tank combination. The lamination method chosen was a double-chamber vacuum laminator using PVB as an encapsulant. Final cycle time on the prototype was 32 min. Development of a carousel containing a number of these laminators was proposed, but was not pursued.

Use of in-line solder flux cleaning raised the question of corrosive flux residues. An in-house experiment at JPL showed that adequate solder flux removal required a heated ultrasonic bath followed by a vapor degreaser rinsing. Two baths are needed to maintain output quality and to cope with the polar and non-polar solubles present in solder flux and flux residues, respectively.

Kulicke and Soffa is noted for its line of automated semiconductor assembly equipment. Their concern was to build an automated cell inter-connection machine that would satisfy the needs of the entire PV industry (Reference 99). The cell interconnection and module lay-up processes were automated with the operator primarily performing only cassette loading and semi-finished module unloading (Figure 44). Pulse bonding was used to solder the cell interconnects. A walking beam mechanism was used to move the cells during stringing and a vacuum lance moved the completed strings. Machine cycle time was 5 s/cell.

Motorola, Inc. continued with their AR coating studies by looking more closely at acid etching processes (Reference 100). The selected process used a fluosilicic acid solution saturated with silica to attack the surface of soda-lime glass. The resulting film had excellent optical properties and was resistant to soiling and staining. Low resistance to mechanical abrasion and some glass cleaners were problems along with process control.

Soldering cell interconnections creates a flux-cleaning problem and a subsequent solvent disposal problem. Westinghouse R&D Center was concerned with this problem as well as assembly of their 0.006-in.-thick dendritic web cells (Reference 101). Kulicke and Soffa, working on a subcontract, used their previous experience to construct a machine that would ultrasonically bond eight tabs from an interconnect in just 3.5 s. Handling of the thin cells was essentially flawless, and there were no flux contamination concerns. Cell breakage was minimized by using boron instead of aluminum to form the BSF. The completed modules were laminated using a new material, EVA. This material was preferred because it had a lower cost and fewer processing difficulties than PVB.

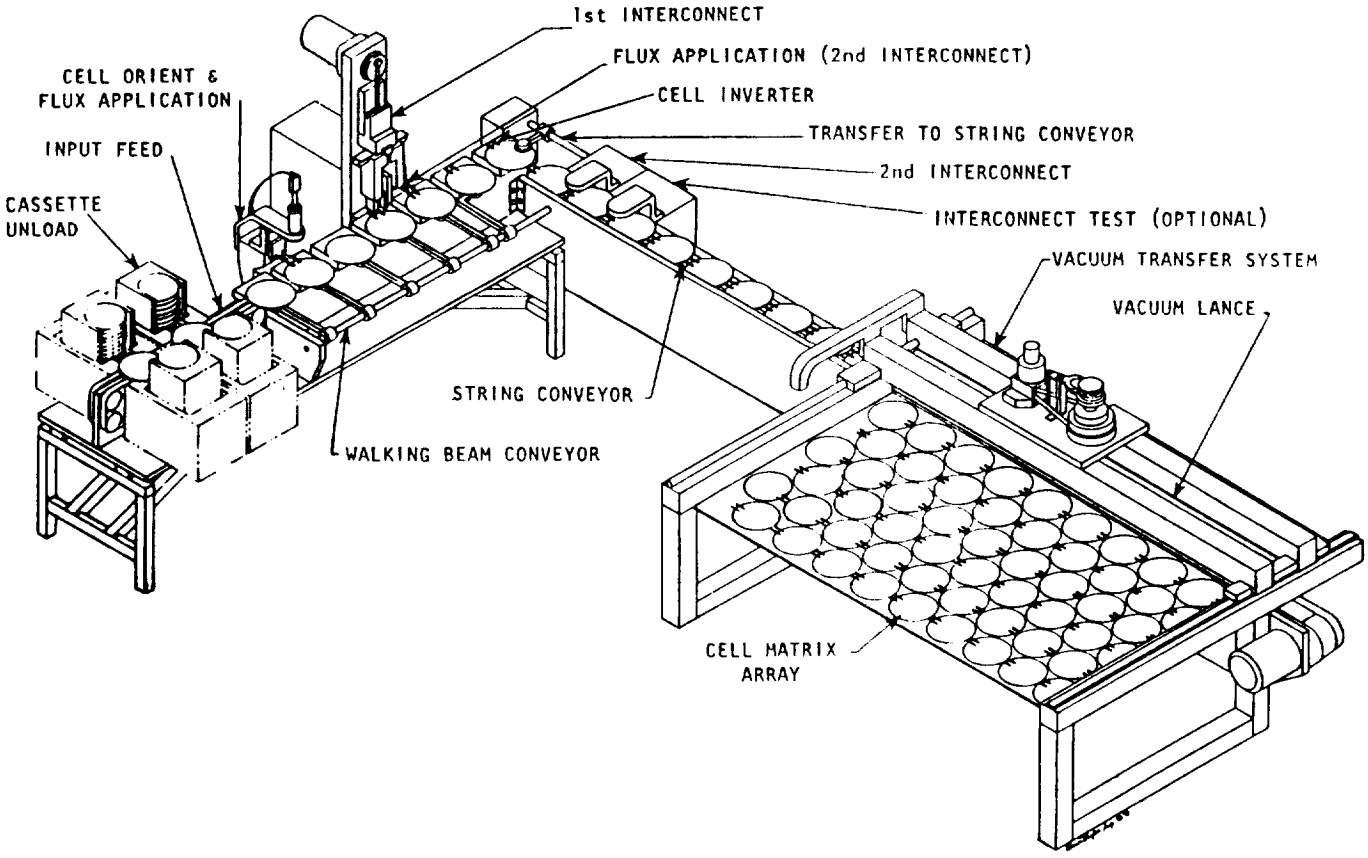


Figure 44. Automated Solar Module Assembly Line

Although cell interconnection and lamination are the most critical assembly processes, they are not the only ones with a high labor content. The Process Development Area worked with the JPL Robotics Group to develop an automated module connector process. The robot used a vision system to locate and verify presence of two copper bus bars on the back of a laminated module. A T-shaped copper tab was grabbed by the end effector, dipped in solder flux, induction heated, and soldered to one copper bus bar. While the end effector was getting the second T-shaped tab, the vision system was inspecting and verifying the location of the first one. When the tabs were assembled, the end effector applied a bead of adhesive around the connector area. This operation was also visually monitored to ensure a continuous bead. A specially designed AMP connector was then bonded to the module by the robot.

Problems with encapsulant materials had been expected and the Encapsulation Task of the FSA Project had screened available materials for candidates. EVA had been used for years as a wire insulation, so it had known outdoor performance. After EVA had been selected as one candidate, an in-house processing evaluation was done at JPL (Reference 102). A prototype ARCO Solar laminator was modified to use a resistive heated blanket instead of high-intensity light. This allowed fabrication of modules with opaque substrates as well as the more common transparent superstrate modules. Once a test bed was prepared, controlled process parameter testing was started. Gel percentage, adhesion, and water immersion effects were all tested. Water immersion gave a rapid answer to outdoor delamination potential. Adhesion to glass was improved by working with Dow Corning Corp. to develop special silane primers. Problems with the fiberglass scrim used in modules were resolved by changing to an acrylic binder. Du Pont used their own research facilities to create an acrylic adhesive to bond the Tedlar back cover to EVA.

Further use of robotics in module assembly was developed by Tracor MBA (previously MBAssociates) (Reference 103). The robot end effector was equipped with an induction heating coil so that interconnect soldering would be occurring while a cell was being placed on a module superstrate (Figure 45). Improvements were also made in the lamination and edge sealing equipment previously developed. The final automated assembly

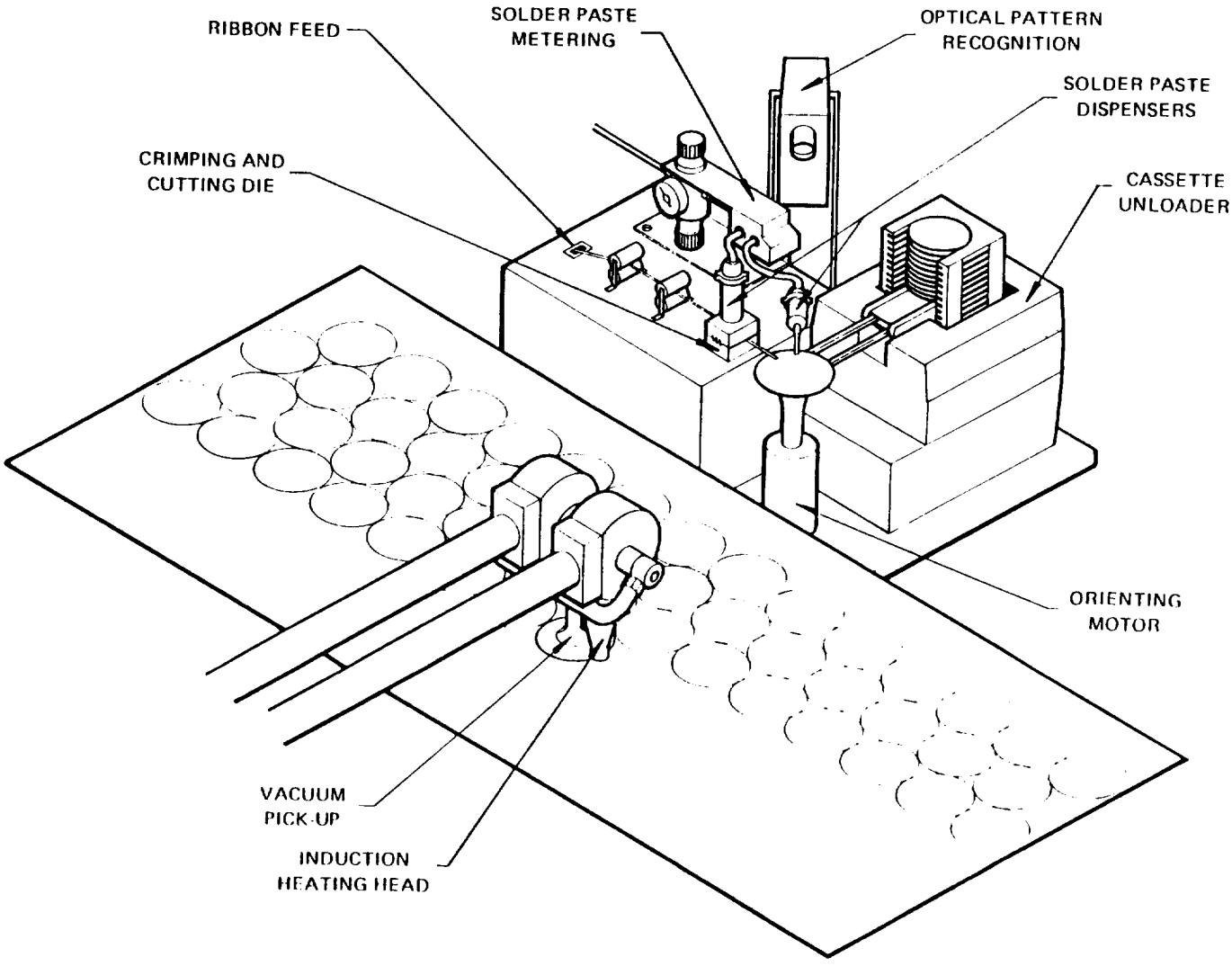


Figure 45. Preparation Station and Panel Lay-Up

module is shown in Figure 46. Other material developments were also included. A glass-reinforced concrete substrate (developed under a different contract) was used for module bonding process development.

The thick-film light-trapping effect, called the "zero-depth concentrator effect" by General Electric, was considered to have economic potential in array design. Science Applications, Inc. made a detailed study of the physics of light-trapping (Reference 104). Favorable efficiency increases (~20%) were found to be achievable. A subsequent economic analysis was not as favorable. Use of high packing factors and very narrow grid lines reduced the available reflected light to a level where special light-trapping efforts were not cost effective.

As the PV program matured, there was considerable interest in developing larger (i.e., 4 x 4 ft) modules. A large module would have less edge loss per area leading to a higher packing factor. Another cost saving is the use of just one terminal box instead of four as required if the common 1 x 4 ft modules were used. This interest led to a JPL effort to develop a large area laminator (Reference 105). Development costs were reduced by use of industry available parts, such as hemispherical pressure tank ends for the housing (Figure 47). This equipment was used by PV industry companies for some of their module and process development work.

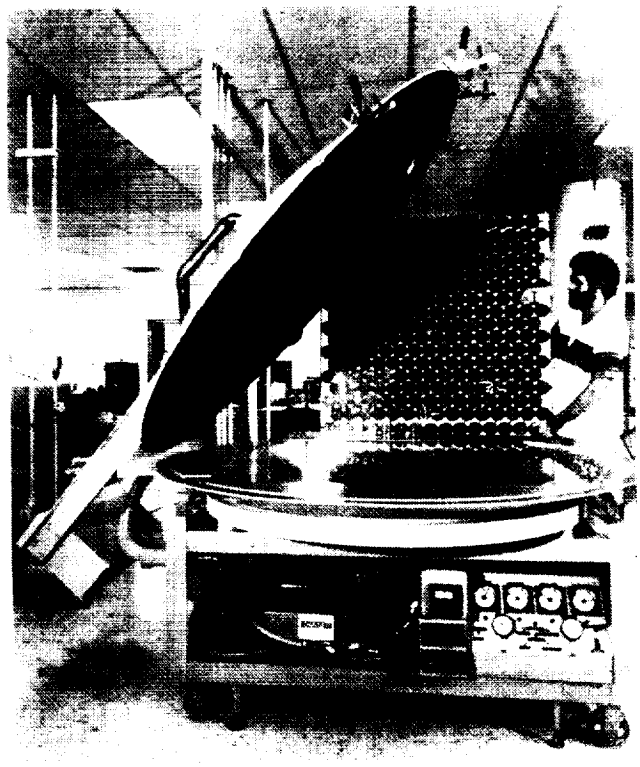


Figure 47. Laminator Module, 4 x 4 ft

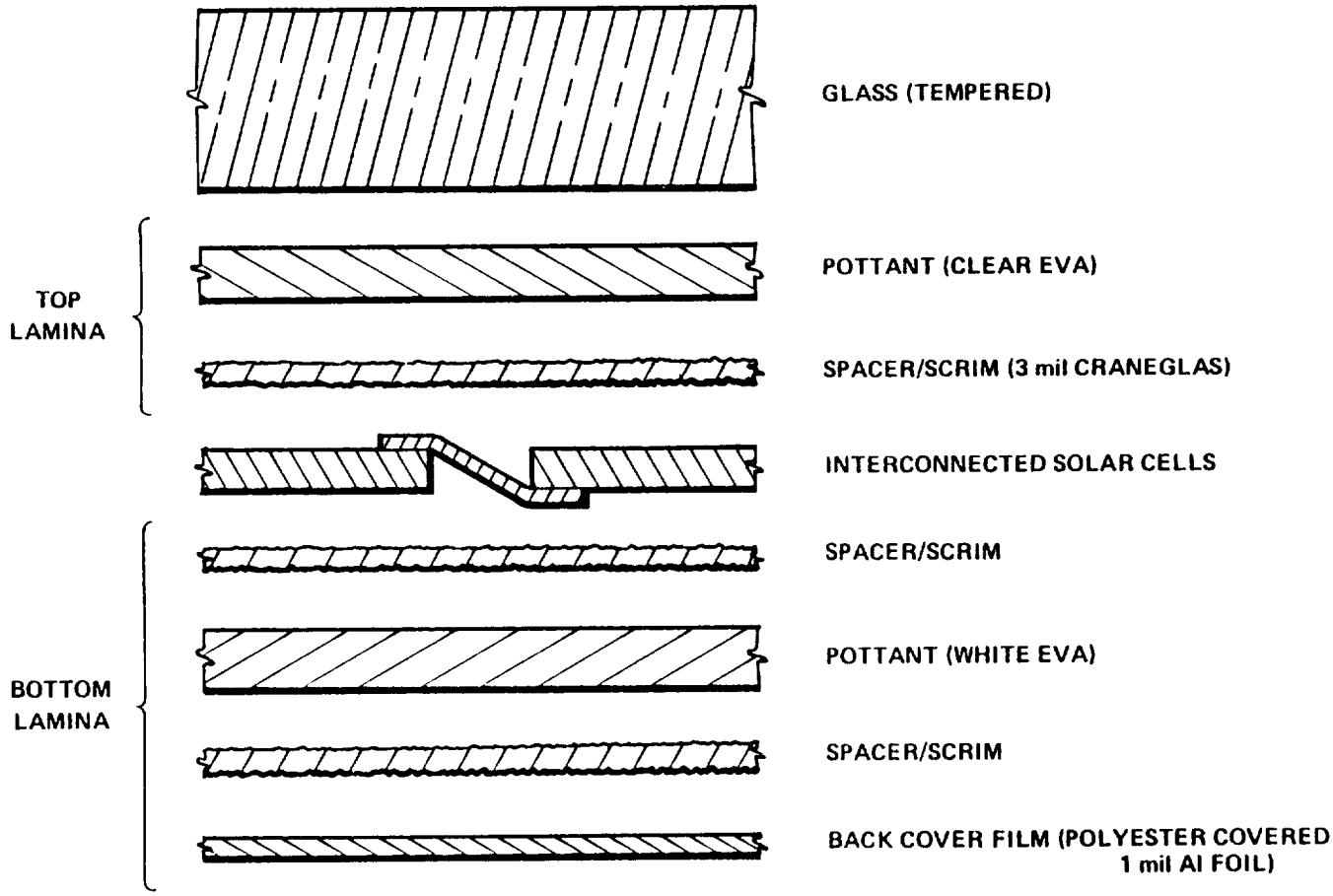


Figure 46. Laminate Composition

Field experience showed that a hermetically sealed module was desirable, and Spire Corp. had specific technology already available for this development (References 85 and 106). Electrostatic bonding (Figure 48) was used to attach an aluminum foil strip around the edge of the module's glass superstrate. Subsequent lamination processing included a back cover with an aluminum foil inner surface (Figure 49). The two aluminum surfaces were joined together by ultrasonic bonding to form a hermetic seal.

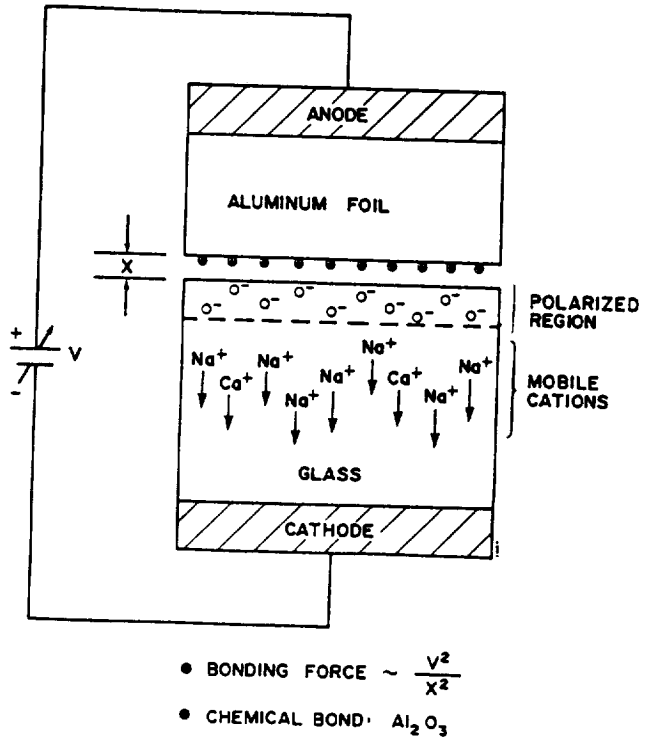


Figure 48. Electrostatic Bonding Process

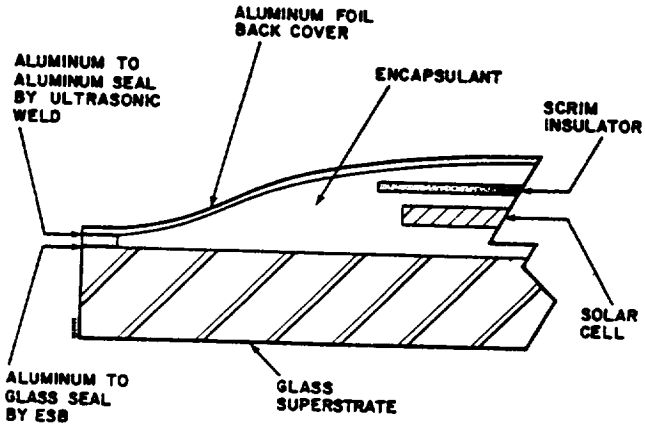


Figure 49. Glass Superstrate Design Module with Aluminum Foil Back Cover and Hermetic Edge Seal

E. RELIABILITY

Reliability of space-borne PV modules was a well-researched subject in 1975 (Reference 107). Terrestrial PV modules had to face an entirely different environment and have an expected life of 20 years. Encapsulation material development and reliability were covered by the Encapsulation Task as part of the FSA Project effort. Reliability of interconnections and electrochemical corrosion were covered by the Engineering Sciences Task and the Module Reliability Task, respectively. The Process Development Task cooperated with these ancillary efforts. Direct concerns of the Process Development Area were: mechanical yield (such as cell and cells string handling) and process yield, especially in interconnection and lamination.

Automation of the cell interconnection process achieved significant improvement in cell handling and interconnect bond reliability. Westinghouse dendritic cells only 0.006 in. thick were coin stacked as input to the Kulicke and Soffa equipment. This process handled these fragile cells at a rate of one every 3.5 s with a mechanical yield of at least 99.9% and an ohmic interconnect yield of 100%. (This electrical yield is only estimated from mechanical pull tests because there are eight redundant bonds on both the top and bottom of each cell.)

Development of improved encapsulation materials and primers was necessary for good lamination performance. Equally important was the development of the double-chamber vacuum lamination equipment and proper module lay-up and lamination procedures. Present industry lamination yield has been excellent using these FSA-developed materials, processes, and procedures.

F. ECONOMICS

As previously noted, the module materials and assembly cost was about $3/W in 1975. By 1982, the SAMICS estimated costs were within the FSA cost allocation guidelines of $0.30/W (1982 dollars). It was originally planned to verify these costs by running a MEPSDU as a pilot line. This effort was not pursued.

G. KEY ACCOMPLISHMENTS

Improvements in assembly processes, equipment, and materials have been detailed in the prior discussion. A summary of the key achievements is listed below by process:

(1) Cell Interconnection

(a) Fully automated interconnect soldering equipment developed, demonstrated, and being used for volume production of standard 0.012-in.-thick cells.

(b) Fully automated interconnect ultrasonic bonding equipment developed and demonstrated for use with fragile 0.006-in.-thick cells.

(c) Robotic cell interconnection developed and demonstrated.

(2) Cleaning

In-line, ultrasonic, cell-string cleaner developed, demonstrated, and in use for volume production.

(3) Lay-up and Wiring

Automated lay-up equipment developed and demonstrated.

(4) Lamination

(a) Encapsulation material use reduced from 0.375-in.-thick cast silicone down to 0.030-in.-thick EVA. Industry standard practice.

(b) Double-chamber vacuum lamination equipment developed, demonstrated, and being used for volume production. Industry standard practice.

(c) Cooperated in development of glass primers that achieved an expected 20-year module life.

(5) Framing

No specific development effort because this is a low-cost, low-technology process.

(6) Diode and Terminal Wiring

Robotic terminal assembly and inspection.

(7) Testing and Packaging

No specific development effort.

H. CURRENT STATUS

No assembly process development contracts have been awarded since 1981 except for the small hermetic seal effort. All Project milestones on cost, performance, and process rate were met by demonstration. Cost estimates were not verified by pilot production runs because of program redirection.

I. REQUIRED FUTURE TECHNICAL NEEDS

The present emphasis on high-efficiency cell research may result in new cell designs that require special handling or interconnection equipment. Similarly, research and development of thin-film PV devices may require special environmental packaging. The long-term materials evaluation effort focused on PV array needs must be continued after the FSA phaseout. The new 30-year module lifetime goal may not be met with any degree of confidence without a continuing materials program.

SECTION VI

Conclusions

The Process Development Area met its basic objective to develop cell fabrication and module assembly process technologies required to meet the cost and performance goals for terrestrial PV module production. In so doing, low-cost cell and module production processes were identified and developed; equipment and facilities to perform these processes were designed and, in many cases, built; the fabrication of low-cost PV cells and modules was demonstrated; and this production technology was transferred to industry.

Program redirection toward higher-efficiency modules has introduced new process technologies whose cost characteristics, sequence synergisms, and reliability have not been determined.

A. MAJOR ACCOMPLISHMENTS

Improvements in the four major categories of investigation by the Process Development Area have been detailed in previous discussions. A summary of the key achievements by major category is listed below:

(1) Surface Preparation

(a) Studies proved the technological and economic feasibility of automation.

(b) Surface cleanliness found to be critically important in fabricating high-efficiency cells.

(c) Developed test patterns found to be useful process development and monitoring tools.

(d) Industry-standard texturizing process developed.

(e) A complex megasonic cleaning process with the attendant equipment developed and transferred to industry.

(f) A spin drying cycle found to be the preferred drying cycle.

(g) Silicon nitride found to be an excellent multipurpose cell coating that can function as an AR coating, a surface passivant, a metallization pattern mask, and a diffusion barrier.

(2) Junction Formation

(a) Large-area, large-volume gaseous diffusion processes using $POCl_3$, PH_3, and BBr_3 were demonstrated.

(b) Spin-on, spray-on, and meniscus coating processes for volume production were demonstrated.

(c) Simultaneous front and back junction forming processes using liquid dopant and RTP were developed.

(d) NMA ion implementation of both front and back junctions was developed.

(e) Ion implantation equipment capable of rates of 300 wafers per hour was demonstrated, along with laser, pulsed electron beam, and rapid thermal process annealing.

(3) Metallization

(a) Thick-film screenable cost-effective processes using Ag, AgAl, Cu, and MOD AgBi were developed.

(b) Developed reliable plating systems using Pd and Ni followed by either solder build-up by immersion or Cu plating to provide the required conductivity.

(c) MOD films that provide low temperature contact systems ($< 390\,^{\circ}C$) were developed.

(d) Generic fabrication processes for MOD films were developed and the technology was transferred to industry.

(e) Pyrolitic decomposition of MOD films using a laser was developed, further ensuring low bulk substrate temperatures.

(4) Module Fabrication

(a) Fully automated interconnect soldering equipment was developed, demonstrated, and used for volume production.

(b) Fully automated ultrasonic bonding equipment was developed and used for volume production. This is now an industry standard practice.

B. CURRENT STATUS

Although Project milestones on costs, performance, and rates have been demonstrated for the developed processes, described herein, they (costs in particular) have not been verified by pilot runs because of program redirection.

This same program redirection (for high-efficiency modules) has resulted in the investigation of more sophisticated processes to maintain bulk silicon characteristics, reduce surface recombination rates, and improve AR coatings. These processes are still in the development stage and the synergistic effects of their inclusion in the current industry standard process sequences are unknown. Their projected costs in volume production and their long-term reliability have not been determined.

C. FUTURE TECHNICAL NEEDS

The present emphasis on high-efficiency cell research has resulted in the investigation of new, more sophisticated processes than those currently used by industry. The implementation of these processes into existing product lines and the effects on efficiencies, yields, and overall costs must be examined before large-scale production is initiated.

Studies of material interactions in the basic process sequences must be continued if the 30-year reliability goals of the Project are to be realized. As an example, materials used to attain low surface recombination velocities on the cell surface may require special environmental packaging.

SECTION VII

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APPENDIX

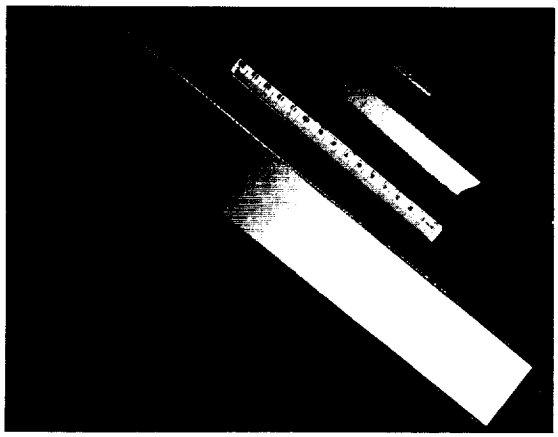
Glossary

AR	antireflective
Al	aluminum
BSF	back surface field
Caltech	California Institute of Technology
CVD	chemical vapor deposition
Cz	Czochralski
DC	direct current
DI	deionized
DOE	U.S. Department of Energy
EDS	energy dispersive spectroscopy
EFG	edge-defined film-fed growth
erfc	complementary error function
ESL	Electro-Science Laboratories, Inc.
EVA	ethylene vinyl acetate
FSA	Flat-Plate Solar Array (Project)
HEM	heat exhange method
IPEG	Interim Price Estimation Guideline
IR	infrared
ITO	indium tin oxide
I-V	current-voltage
JPL	Jet Propulsion Laboratory
LSSA	Low-Cost Silicon Solar Array (Project)
MEPSDU	Module Experimental Process System Development Unit
MOD	metallo-organic decomposition
NMA	non-mass analyzed
PA&I	Project Analysis and Integration
PEBA	pulsed electron beam annealing
PV	photovoltaic(s)
PVB	polyvinyl butyral
RF	radio frequency
RFP	Request for Proposals
RTP	rapid thermal processing
RTV	generic silicone molding compound (General Electric)
SAMICS	Solar Array Manufacturing Industry Cost Standards
SAMIS	Solar Array Manufacturing Industry Simulation
SEM	scanning electron microscope
SOA	state of the art
TDM	Technical Direction Memorandum
UV	ultraviolet
WDS	wave dispersive spectroscopy

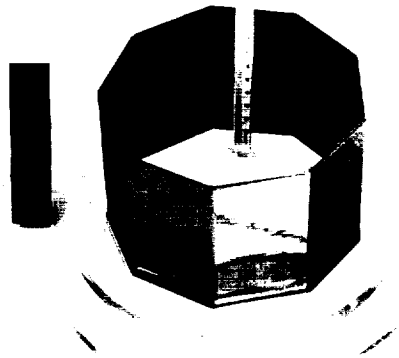
Prepared by the Jet Propulsion Laboratory, California Institute of Technology, for the U.S. Department of Energy through an agreement with the National Aeronautics and Space Administration.

The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and is part of the National Photovoltaics Program to initiate a major effort toward the development of cost-competitive solar arrays.

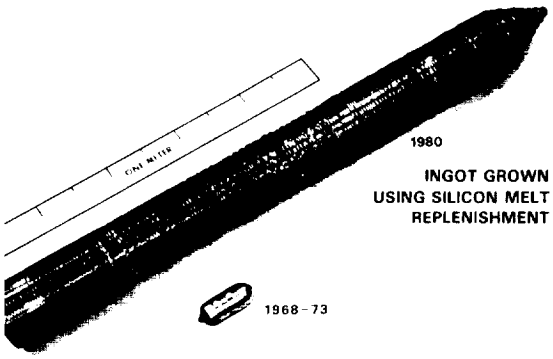
More Technology Advancements



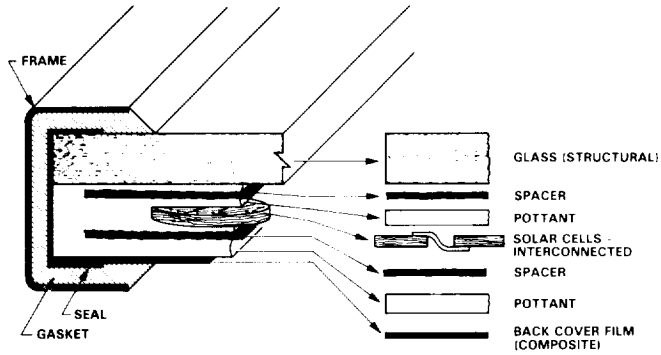
Dendritic web silicon ribbons are grown to solar-cell thickness. Progress is shown by experimental ribbons grown in 1976 and 1978 and a ribbon grown in a Westinghouse Electric Corporation pilot plant.



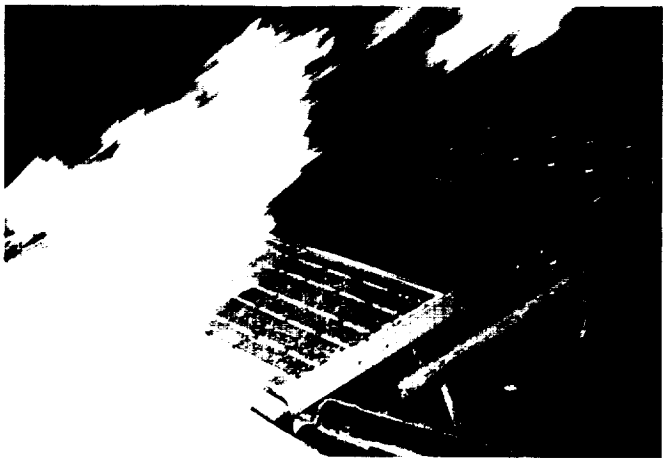
The edge-defined film-fed growth silicon ribbons are grown to solar-cell thickness. A DOE/FSA-sponsored research ribbon grown in 1976 is shown next to a nine-sided ribbon grown in a Mobil Solar Energy Corporation funded configuration.



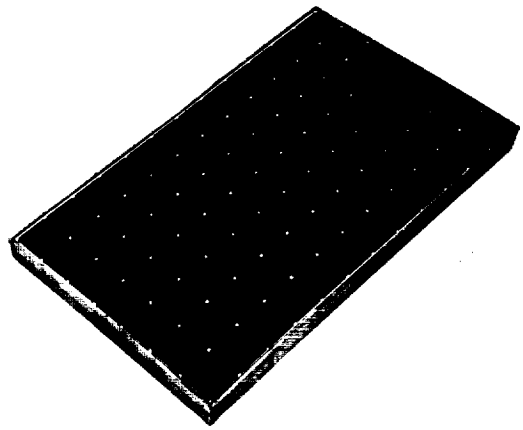
Czochralski silicon crystals as grown are sawed into thin circular wafers. (Support for this effort was completed in 1981.)



Typical superstrate module design is shown with the electrically interconnected solar cells embedded in a laminate that is structurally supported by glass. Materials and processes suitable for mass production have been developed using this laminated design.



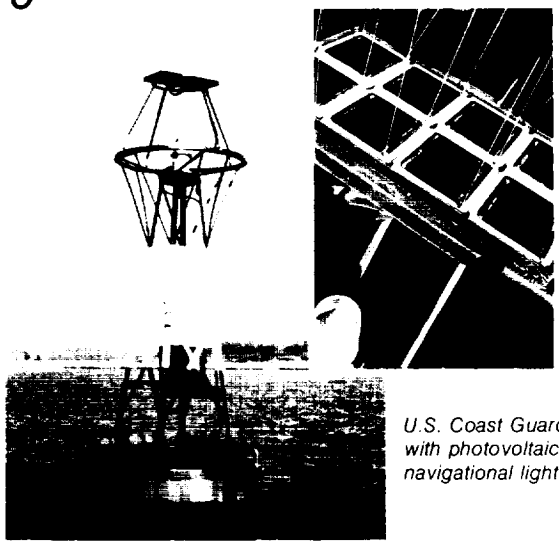
Prototype modules have passed UL 790 Class A burning brand tests which are more severe than this spread of flame test.



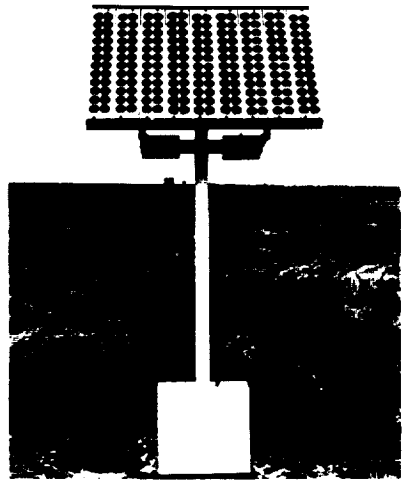
A 15.2% efficiency prototype module (21 x 36 in.) was made by Spire Corp. using float-zone silicon wafers. Recently, similarly efficient modules were fabricated from Czochralski silicon wafers.

Photovoltaic Applications

1975

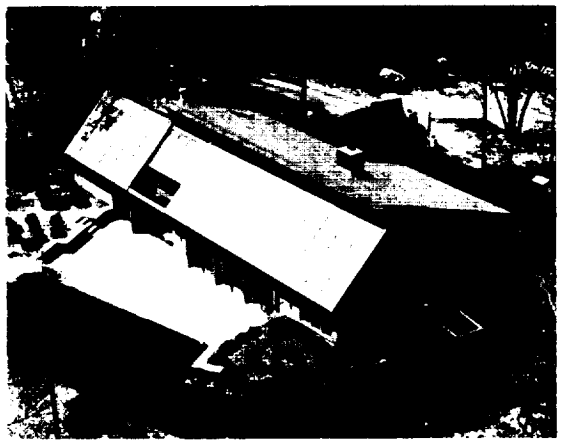


U.S. Coast Guard buoy with photovoltaic-powered navigational light.

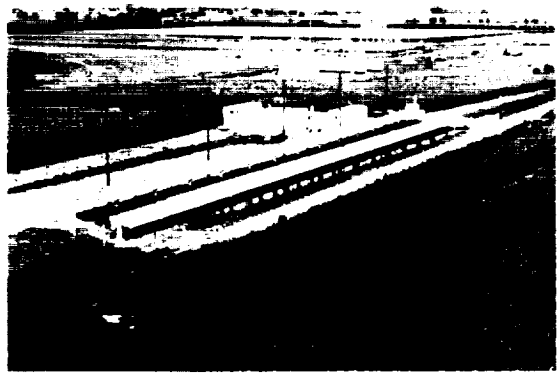


Photovoltaic-powered corrosion protection of underground pipes and wells.

Later...

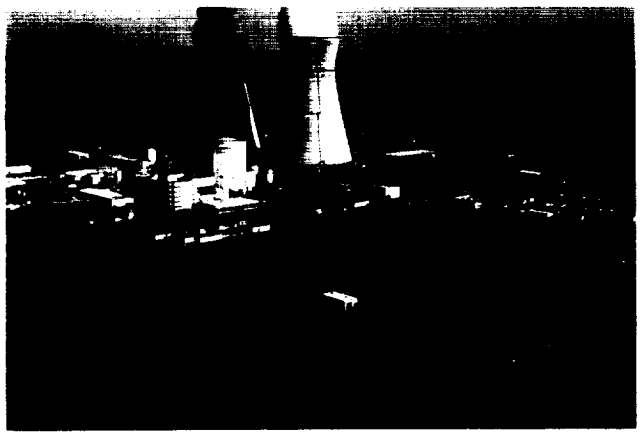


House in Carlisle, Massachusetts, with a 7.3-kW photovoltaic rooftop array. Excess photovoltaic-generated power is sold to the utility. Power is automatically supplied by the utility as needed.



A 28-kW array of solar cells for crop irrigation during summer, and crop drying during winter (a DOE/University of Nebraska cooperative project).

1985



1.2 MW of photovoltaic peaking-power generation capacity for the Sacramento Municipal Utility District. (The 8 x 16 ft panels are mounted on a north-south axis for tracking the sun.)